

**Z96Jm**

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Default	Default
32	PWM0/GPA0	/			GPI
33	PWM1/GPA1	FAN_PWM	O	H	GPI
36	PWM2/GPA2	CLK_PWRSERVE#	O		GPI
37	PWM3/GPA3	/			GPI
38	PWM4/GPA4	CHG_LED_UP#	O	H	GPI
39	PWM5/GPA5	PWR_LED_UP#	O	H	GPI
40	PWM6/GPA6	/	O		GPI
43	PWM7/GPA7	LCD_BACKOFF#	O	H	GPI
153	RXD/GPB0	NUM_LED	O	L	GPI
154	TXD/GPB1	CAP_LED	O	L	GPI
162	GPB2	SCRLED	O	L	GPI
163	SMCLK0/GPB3	SMB0_CLK	SMCLK0		GPI
164	SMDAT0/GPB4	SMB0_DAT	SMDAT0		GPI
5	GA20/GPB5	A20GATE	GA20		GPO
6	KBRST#/GPB6	RC_IN#	KBRST#		KBRST#
165	GPB7	/	I		GPI
47	CLKOUT/GPC0	/	O		GPI
169	SMCLK1/GPC1	SMB1_CLK	SMCLK1		GPI
170	SMDAT1/GPC2	SMB1_DAT	SMDAT1		GPI
171	GPC3	MAIL_LED	O	L	GPI
172	TMRI0/WUI2/GPC4	/	I		GPI
175	GPC5	OP_SD#	O	H	GPI
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I	H	GPI
1	CK32KOUT/GPC7	/			GPI
26	RI1#/WUI0/GPD0	SUSB#	I		GPI
29	RI2#/WUI1/GPD1	SUSC#	I		GPI
30	LPCRST#/WUI4/GPD2	PLT_RST#	LPCRST		LPCRST
31	ECSC#/GPD3	EXT_SC#	ECSC#	H	GPI
41	GPD4	RF_ON_SW#	O	H	GPI
42	GINT/GPD5	/			GPI
62	TACH0/GPD6	FAN0_TACH	TACH0		GPI
63	TACH1/GPD7	/			GPI
87	ADC4/GPE0	DISTP_SW#	I		GPI
88	ADC5/GPE1	/			GPI
89	ADC6/GPE2	EMAIL_SW#	I		GPI
90	ADC7/GPE3	EXPLORE_SW#	I		GPI
2	PWRSW/GPE4	PWR_SW#	PWRSW		GPI
44	WUI5/GPE5	/			GPI
24	LPCPD#/WUI6/GPE6	LID_EC#	I		GPI
25	CLKRUN#/WUI7/GPE7	/			GPI
110	PS2CLK0/GPF0	/			GPI
111	PS2DAT0/GPF1	/			GPI
114	PS2CLK1/GPF2	/			GPI
115	PS2DAT1/GPF3	/			GPI
116	PS2CLK2/GPF4	TP_CLK	PS2CLK2		GPI
117	PS2DAT2/GPF5	TP_DAT	PS2DAT2		GPI
118	PS2CLK3/GPF6	/			GPI
119	PS2DAT3/GPF7	INTERNET#	I		GPI
113	FA16/GPG0	FA16	FA16		GPI
112	FA17/GPG1	FA17	FA17		GPI
104	FA18/GPG2	FA18	FA18		GPI
103	FA19/GPG3	/			GPI
3	FA20/GPG4	THRM_CPU#	I	H	GPI
4	FA21/GPG5	/			GPI
27	LPC80HL/GPG6	PMTHERM#	O	H	GPI
28	LPC80LL/GPG7	AC_APR_UC#	I	H	GPI

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2 )
SO-DIMM 0	1010000x ( A0 )
SO-DIMM 1	1010001x ( A2 )
Thermal Sensor	0100110X ( 98 )

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	B
1394	AD17	0	A
LAN	AD23	2	C

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQE#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	O	Core(To:3.3V)	GPI
E21	GPIO08	EXTSM#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SC#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16/DPRSLPVR	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PC#	STP_PC#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	O	V_CPU_IO	Native



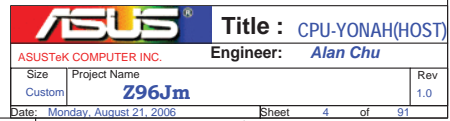
Title : <Title>

ASUSTek Computer INC.

Engineer: Alan Chu

SizeProject Name  
CustomZ96Jm

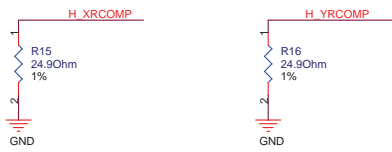
Date: Monday, August 21, 2006Sheet 2 of 91Rev 1.0





## RCOMP

For Calibrating the FSB I/O Buffer



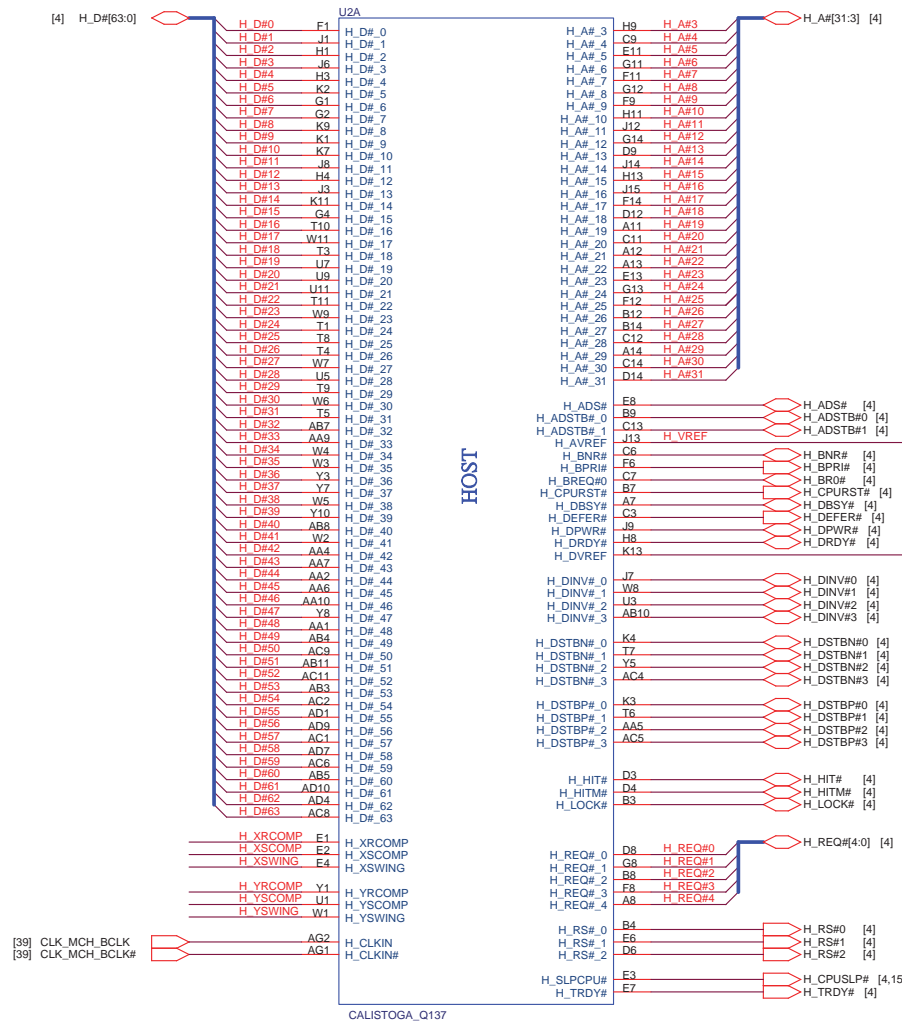
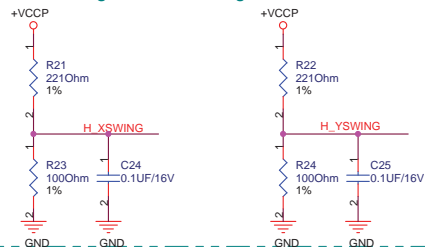
## SCOMP

For Slew Rate Compensation on the FSB

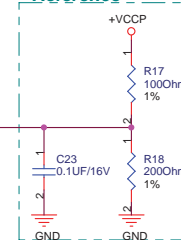


## Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits



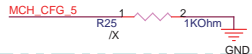
## AGTL+ I/O Voltage Reference



## GMCH Strapping

### CFG5 : DMI Strap

0 = DMI x2  
1 = DMI x4 (D)

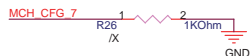


### CFG[13:12] : GMCH Test Mode

00 = Partial CLK Gating Disable  
01 = XOR Mode Enable  
10 = All Z Mode Enable  
11 = Normal Operation (D)

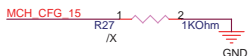
### CFG7 : CPU Strap

0 = DT/Transpotable CPU  
1 = Mobile CPU (D)



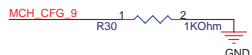
### CFG15 : ICH RESET Disable

0 = ICH Reset Disable  
1 = Normal Operation (D)



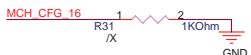
### CFG9 : PCIE Graphic Lane

0 = Reverse Lane  
1 = Normal Operation (D)



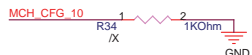
### CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable  
1 = Dynamic ODT Enable (D)



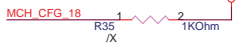
### CFG10 : HOST PLL VCO Select

0 = Reserved  
1 = Mobility (D)



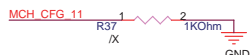
### CFG18 : VCC Select

0 = 1.05V (D)  
1 = 1.5V



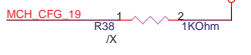
### CFG11 : PSB 4x CLK Enable

0 = 4x Enable  
1 = 8x Enable (D)



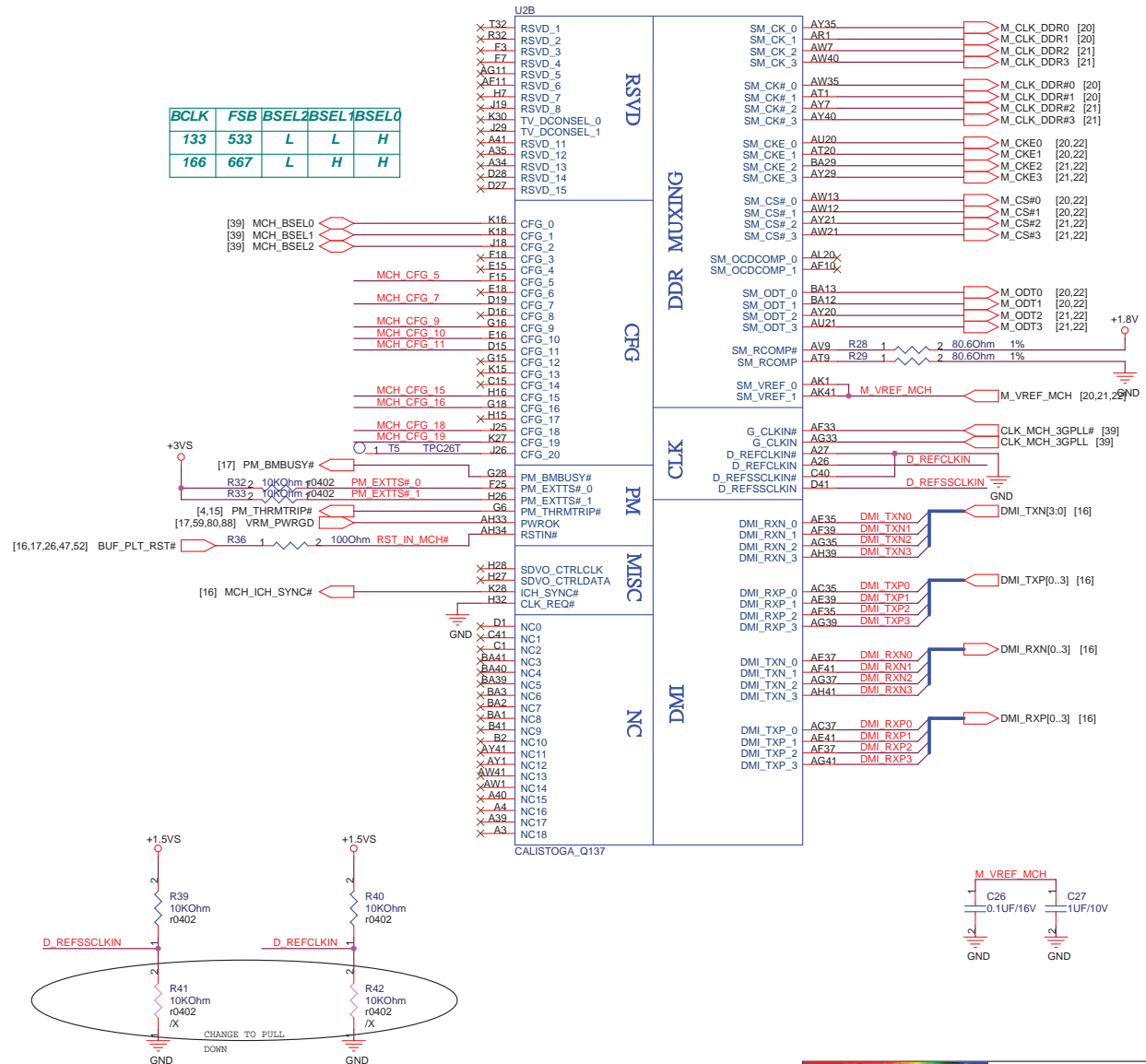
### CFG19 : DMI Lane Reversal

0 = Normal Operation (D)  
1 = Lanes Reversed

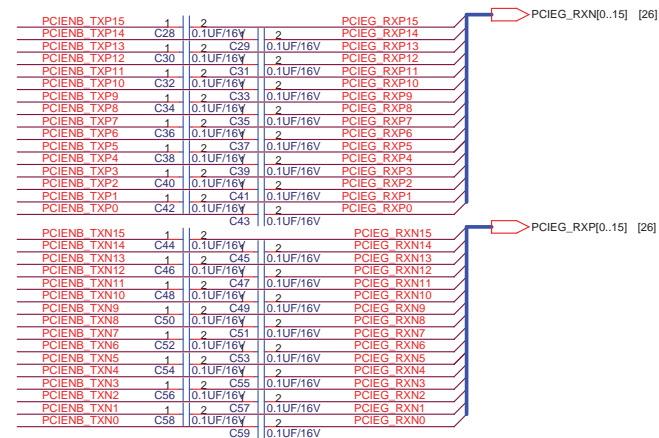
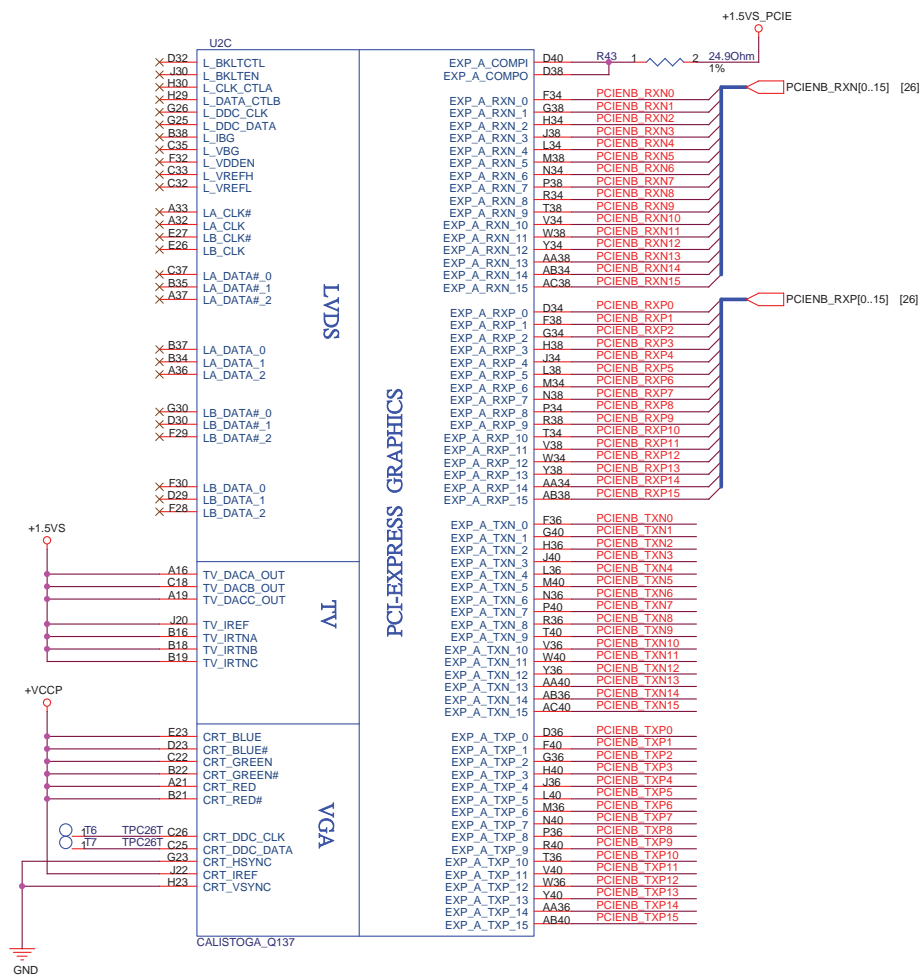


Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

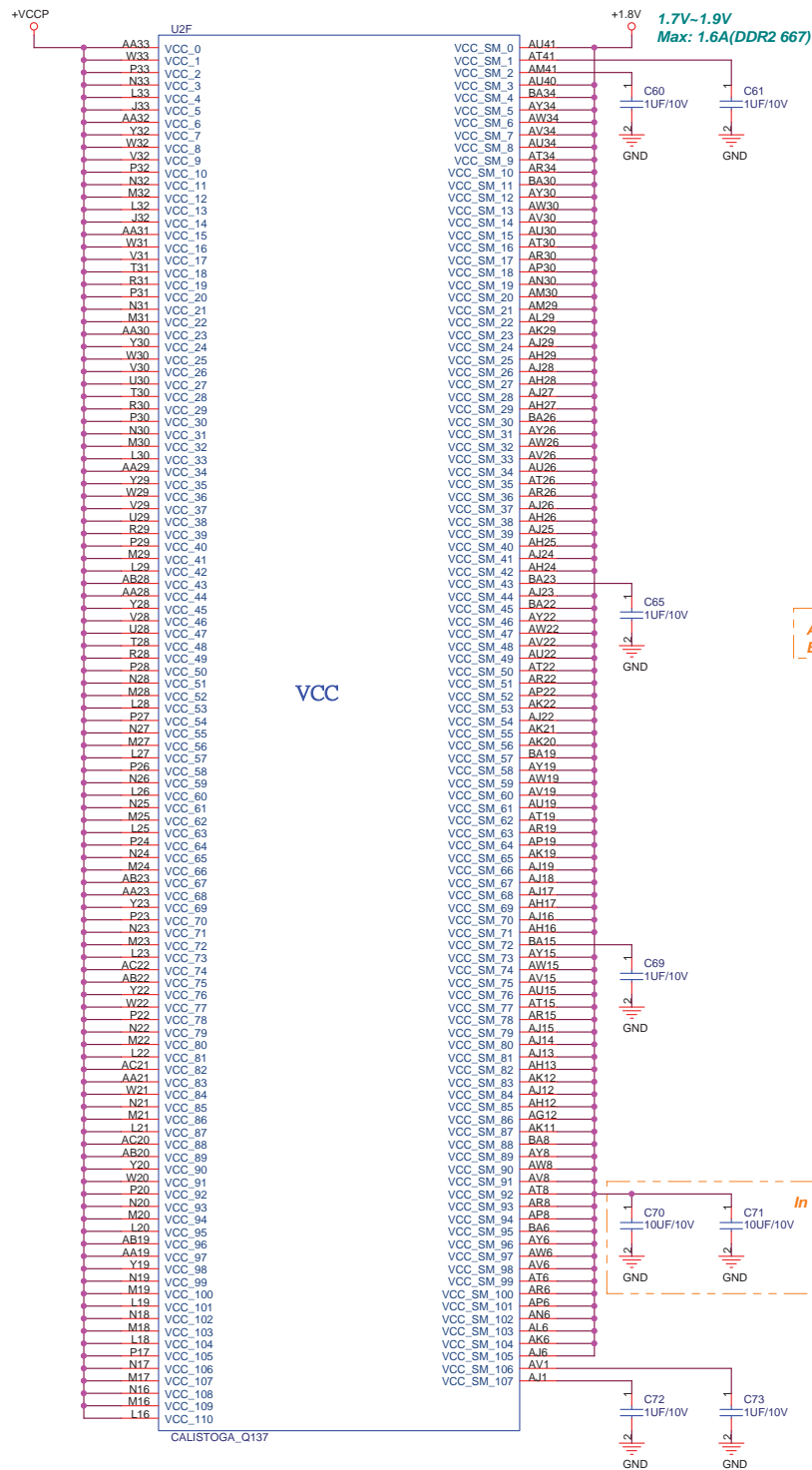




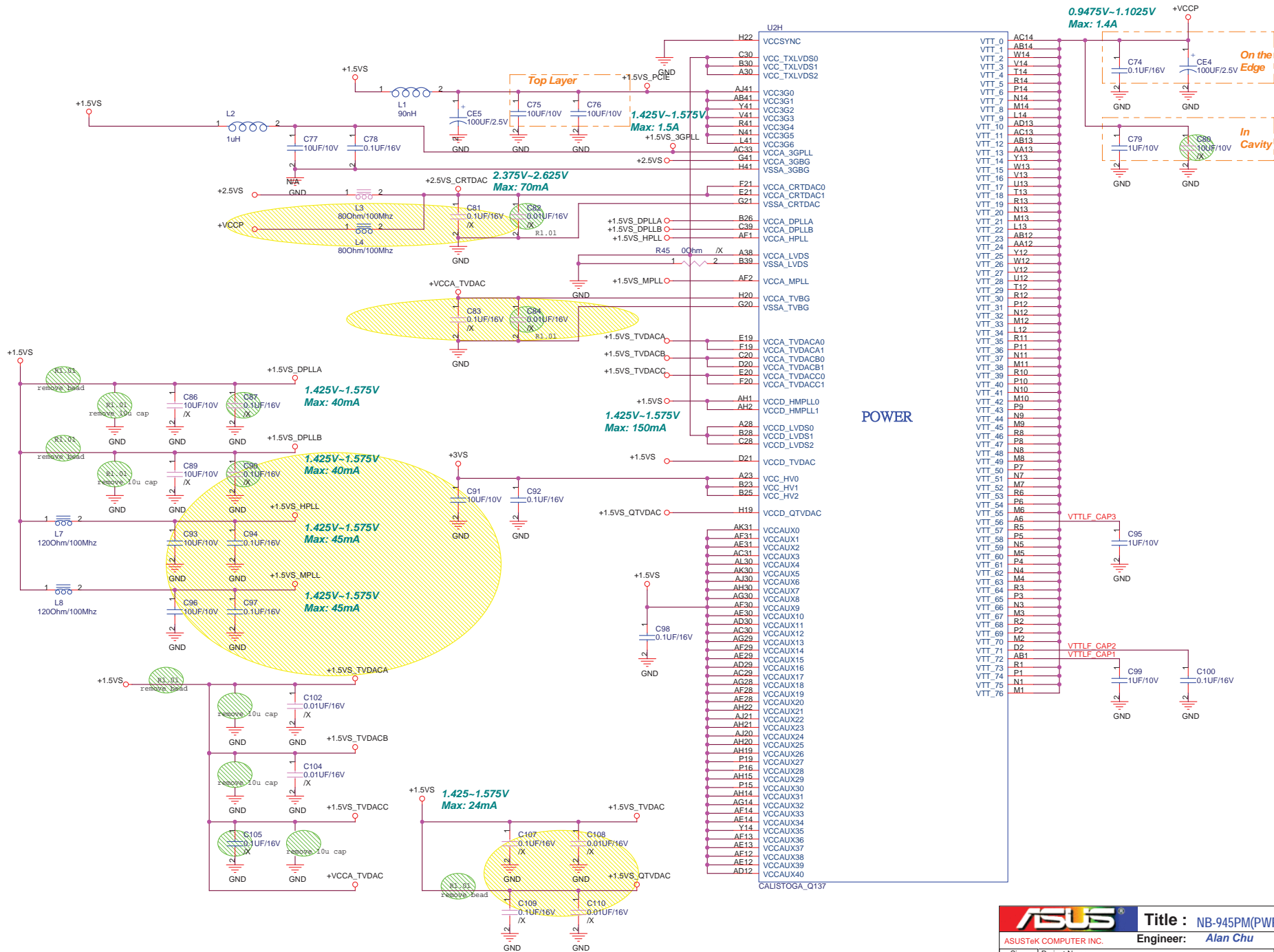


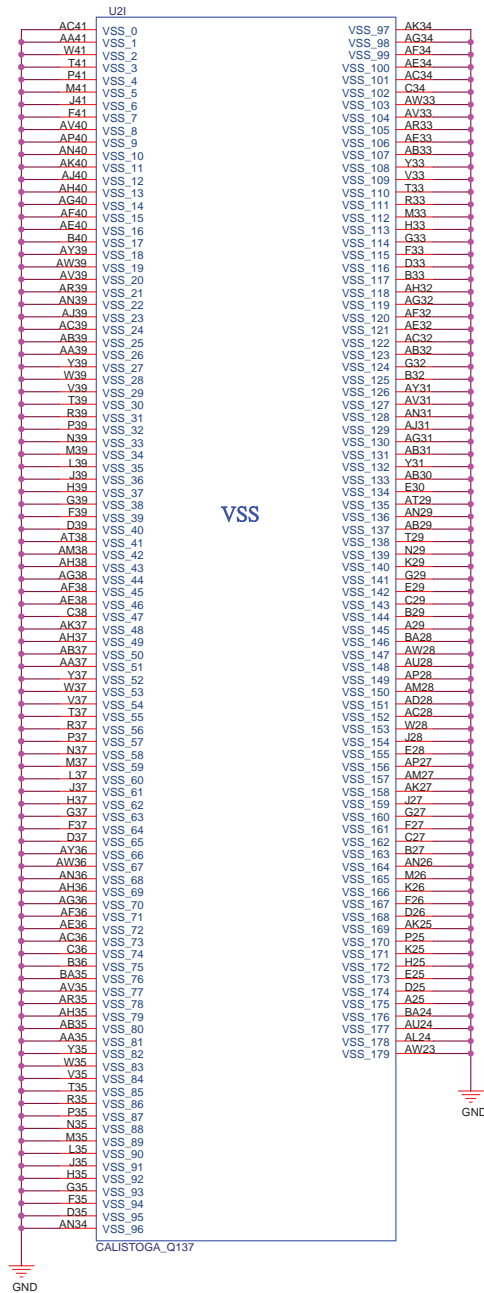


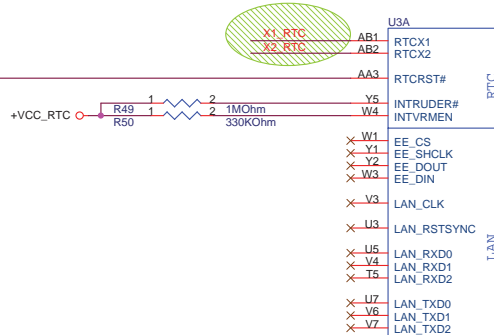
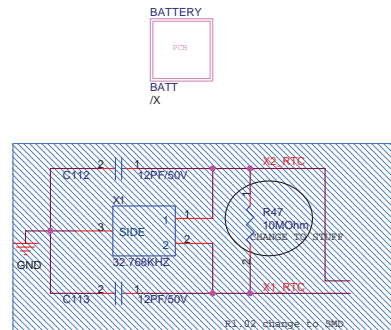




<http://hobi-elektronika.net>

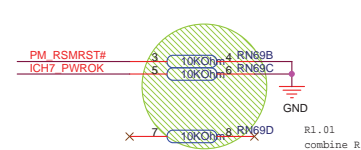
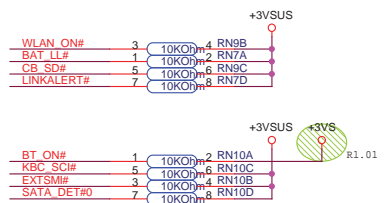
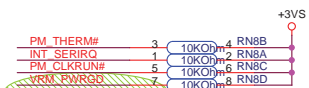
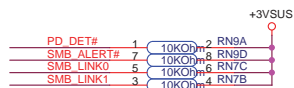
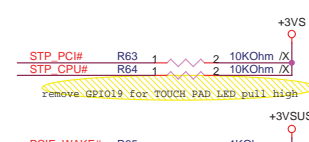
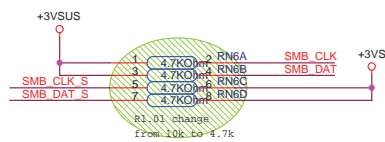
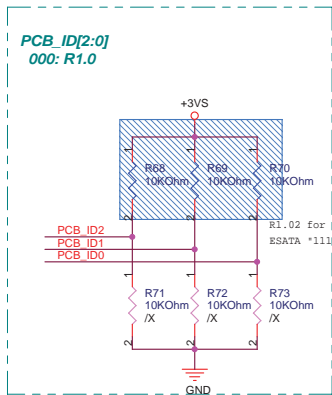
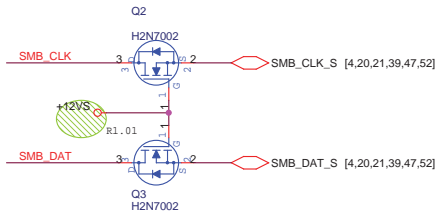
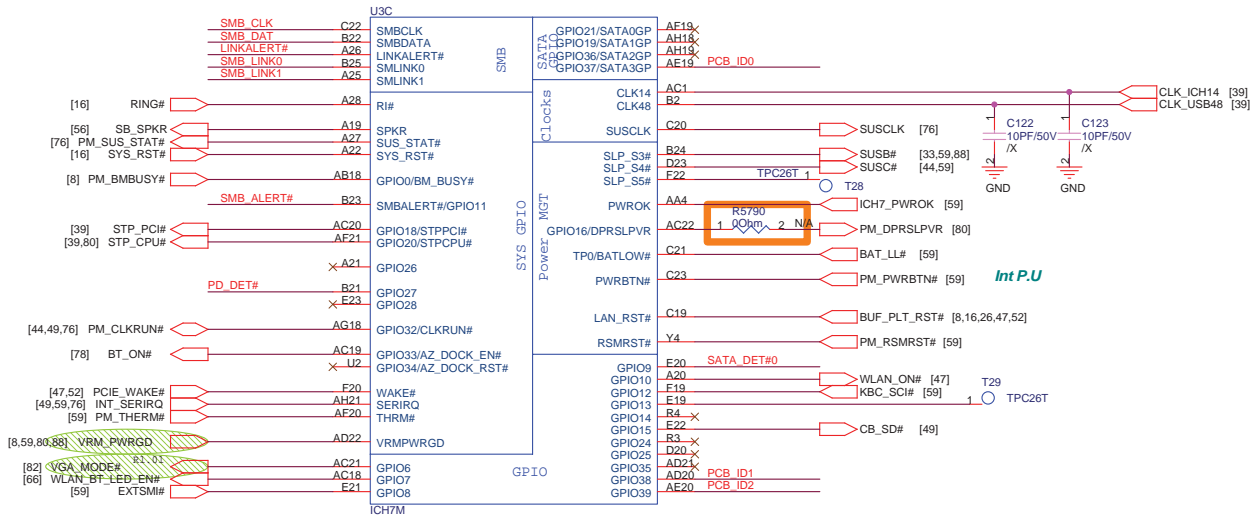








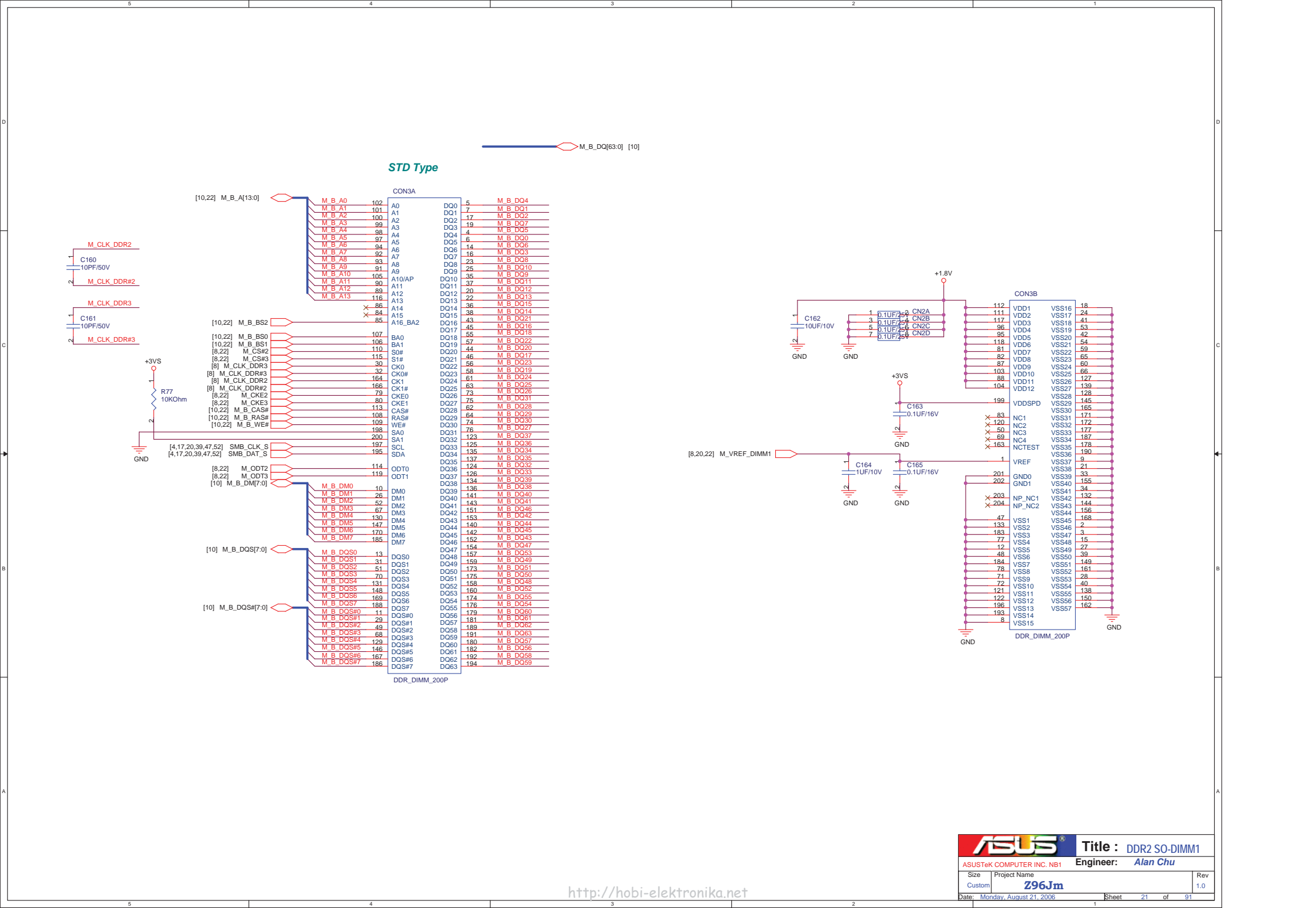
R1.01 add VGA mode select  
 GPU\_VID = 1; Battery Mode ; +1.15V0 = 1.055V  
 GPU\_VID = 0; Performance Mode ; +1.15V0 = 1.158V

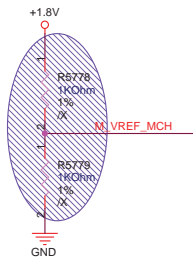




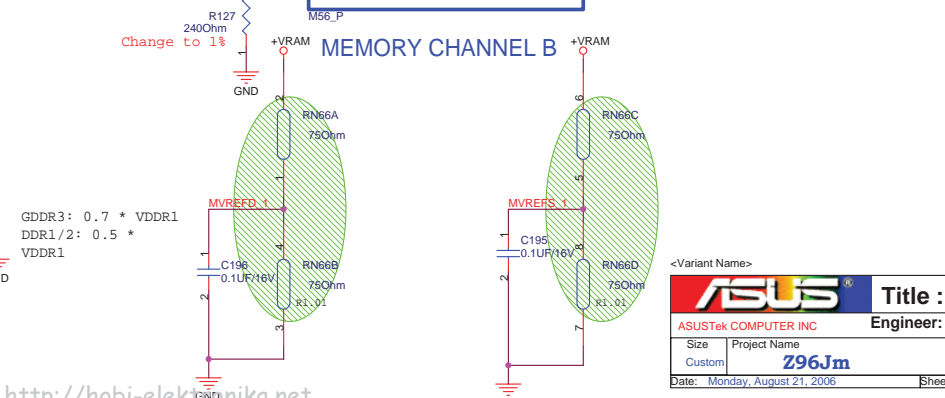
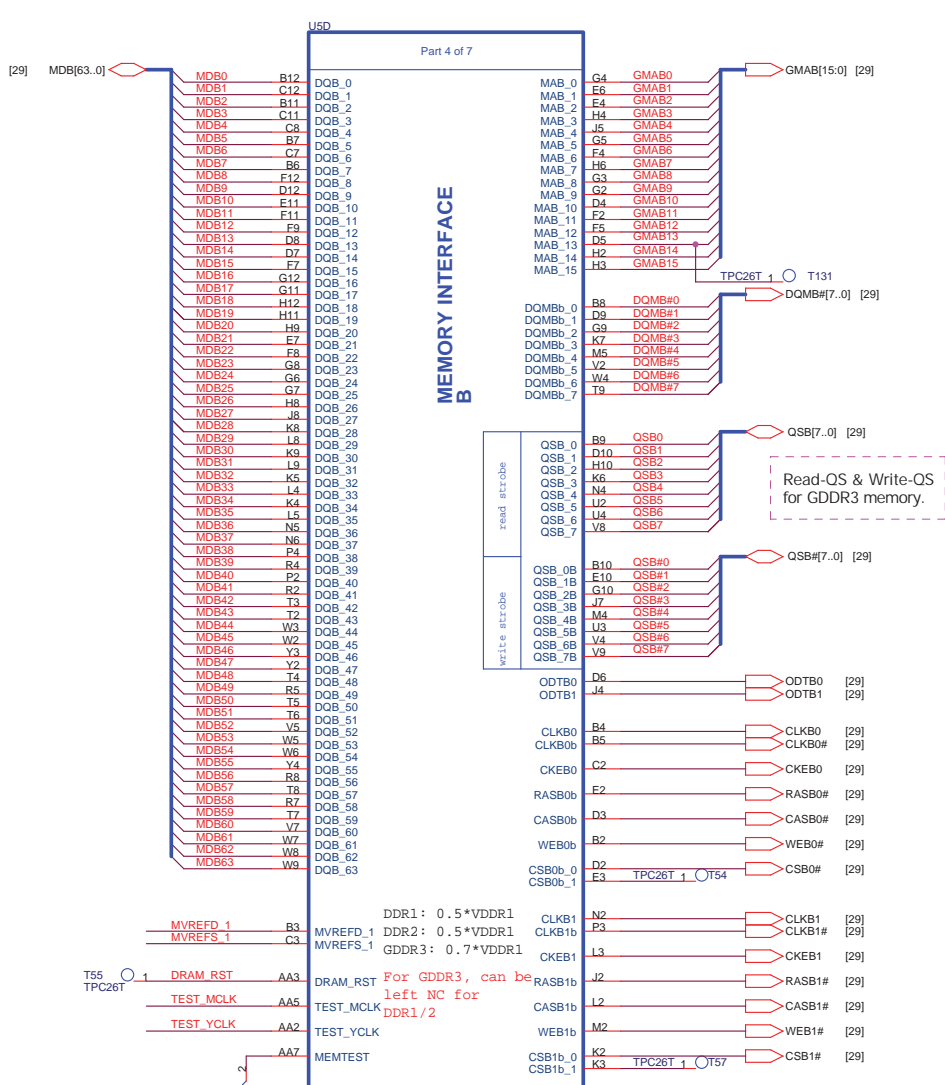
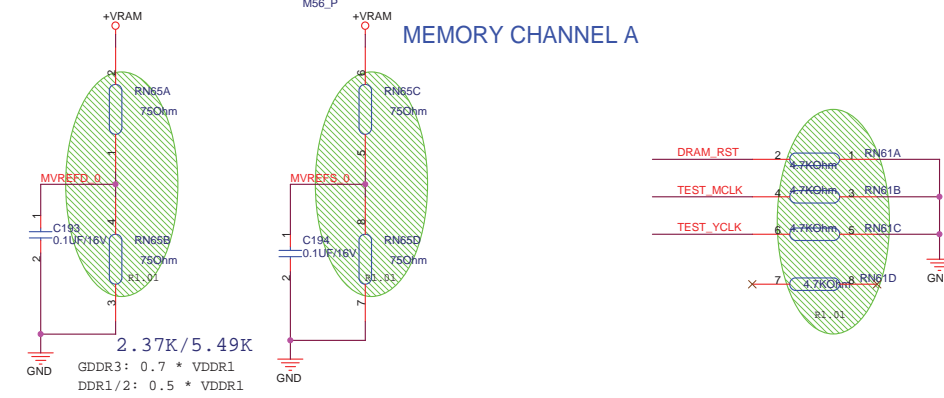
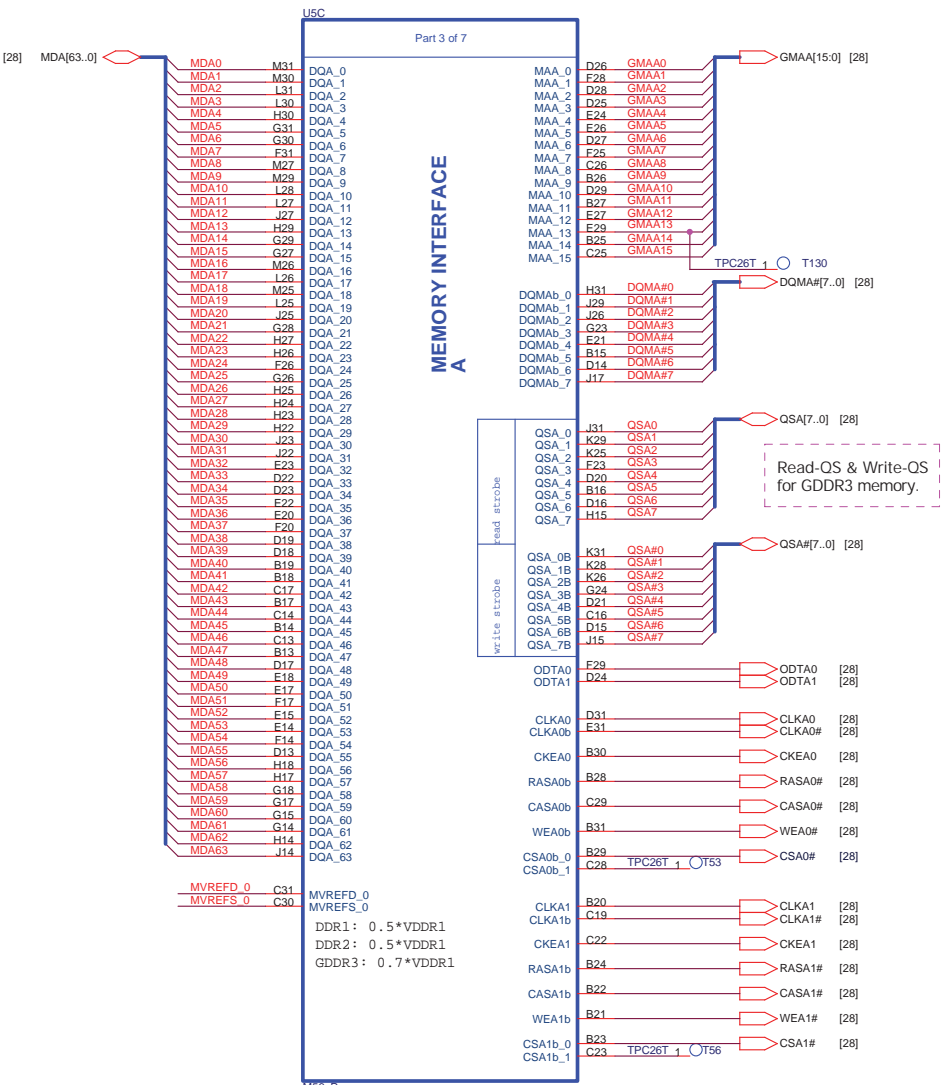






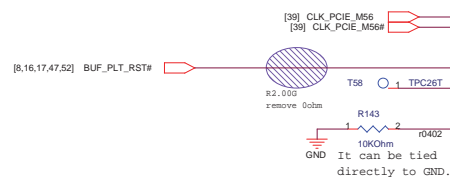


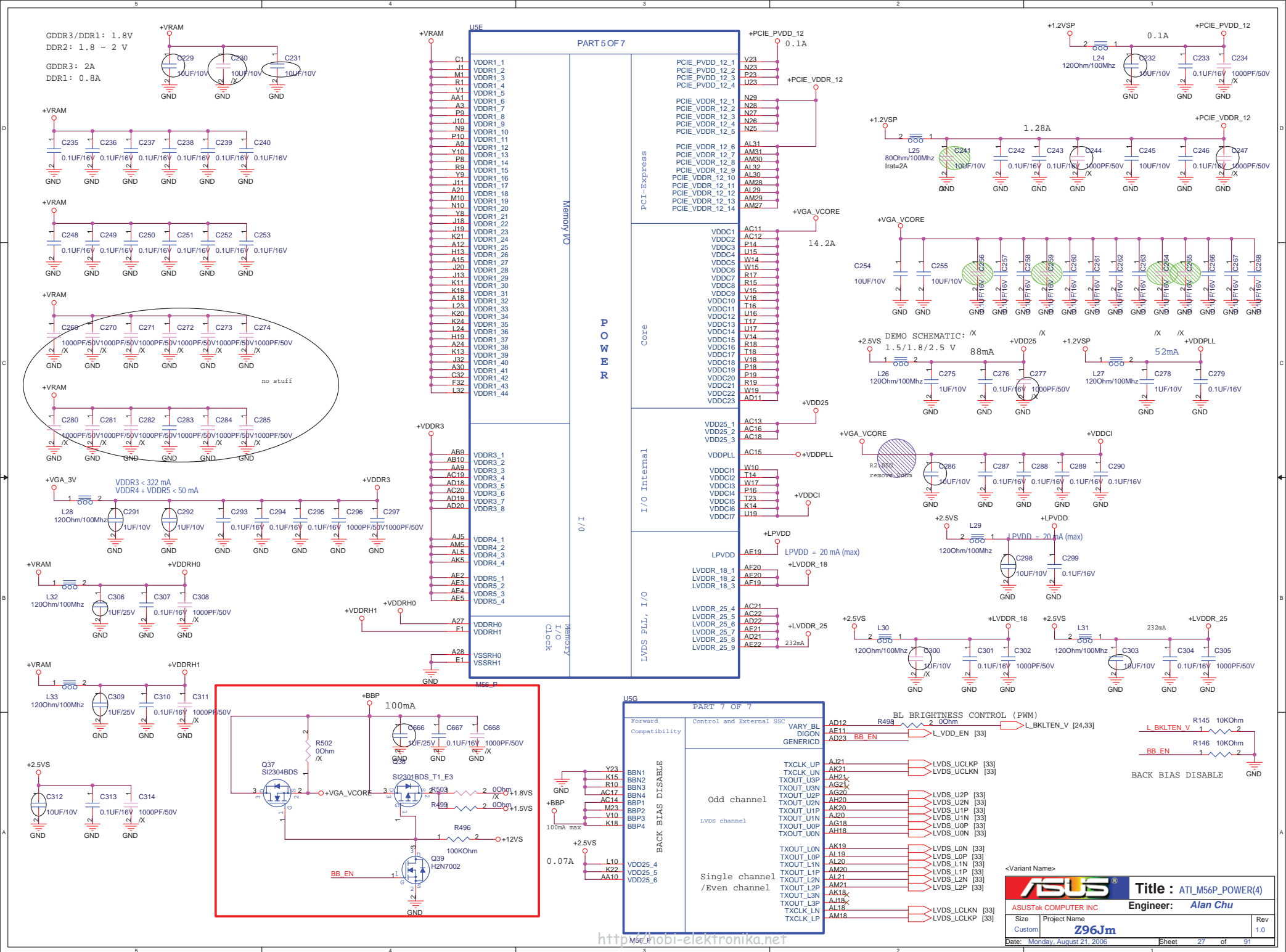


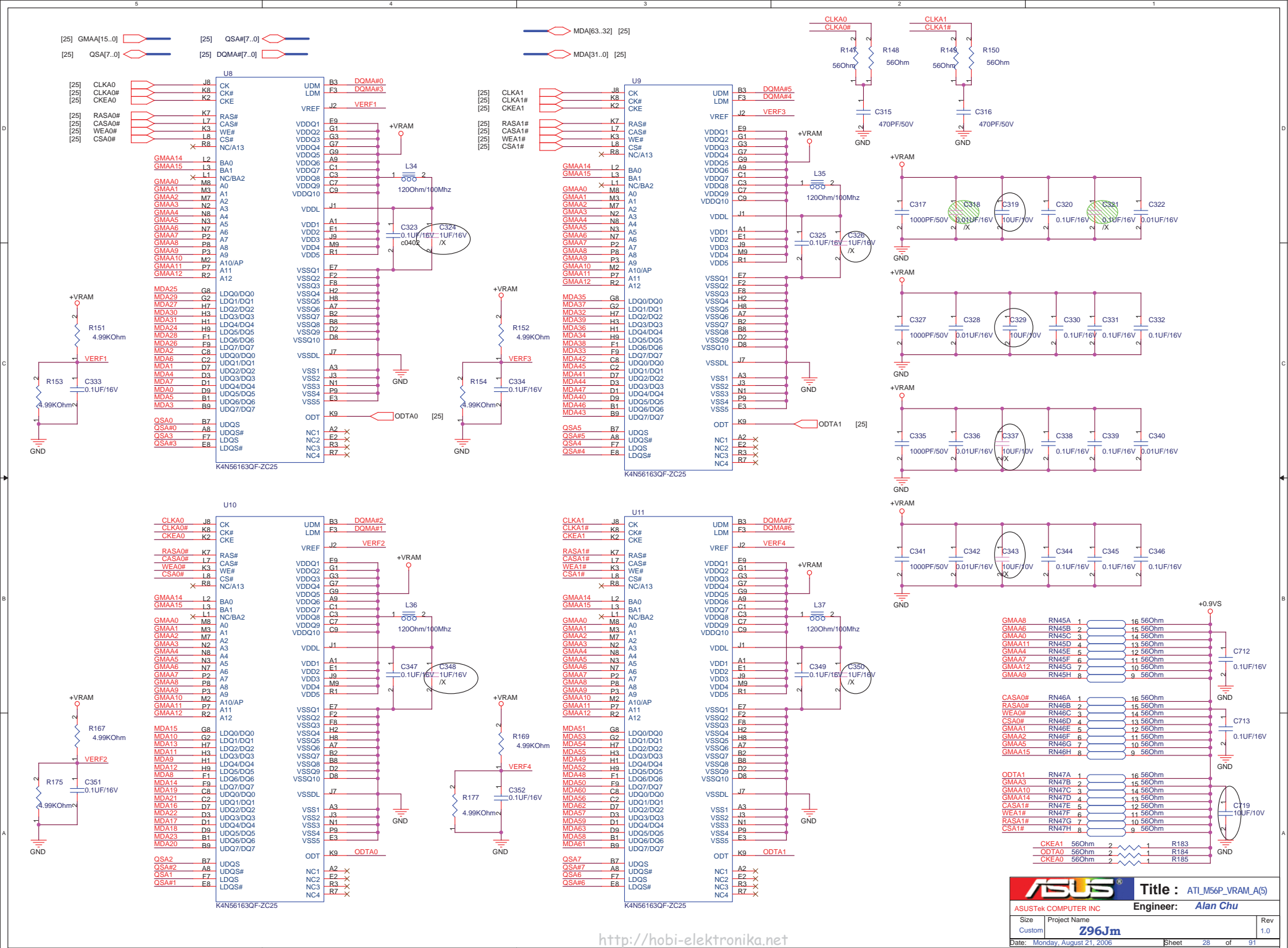


ASUS  
ASUSTek COMPUTER INC  
Size: Custom  
Project Name: Z96Jm  
Date: Monday, August 21, 2006  
Title: ATL\_M56P\_Memory(3)  
Engineer: Alan Chu  
Rev: 1.0  
Sheet: 25 of 91

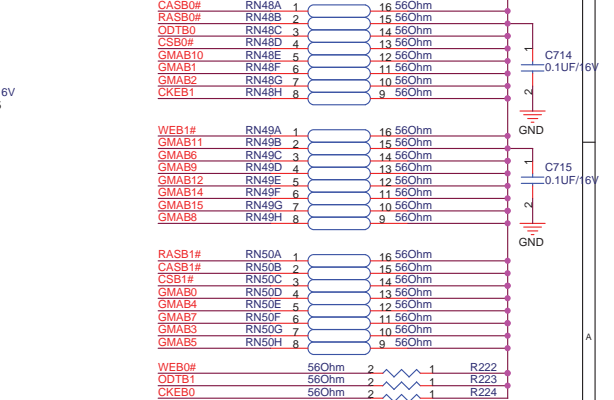
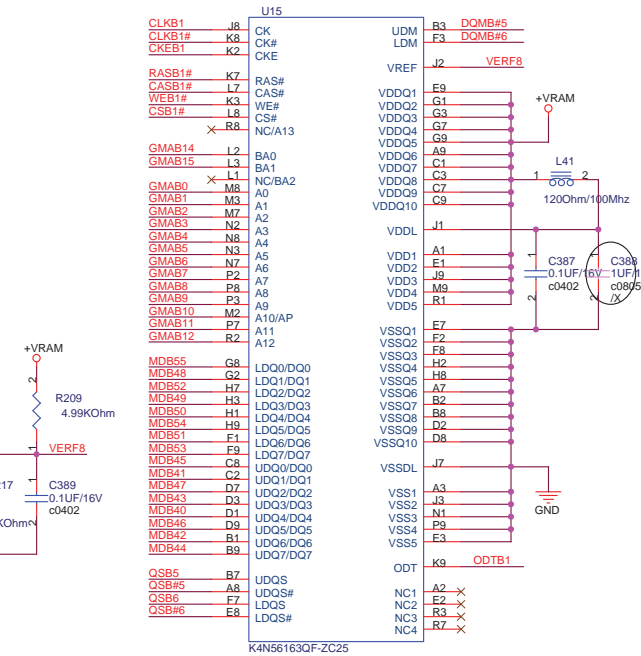
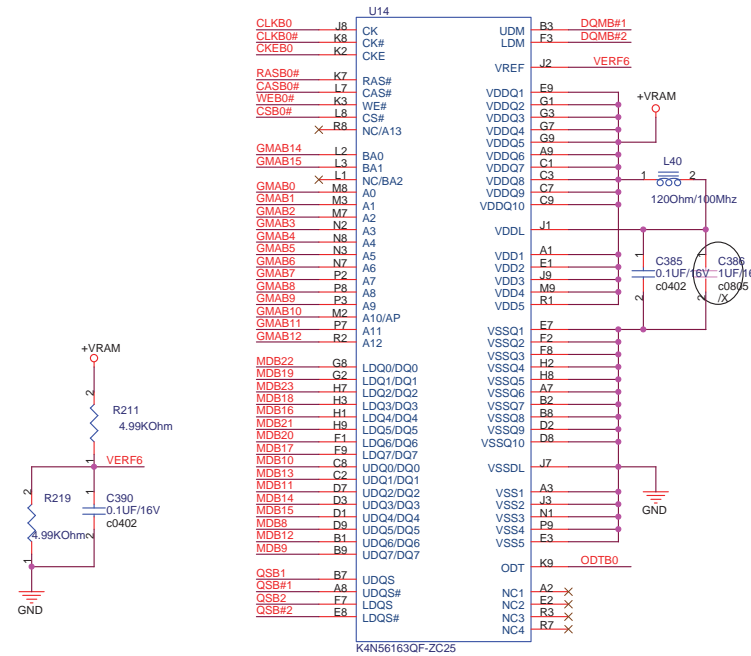
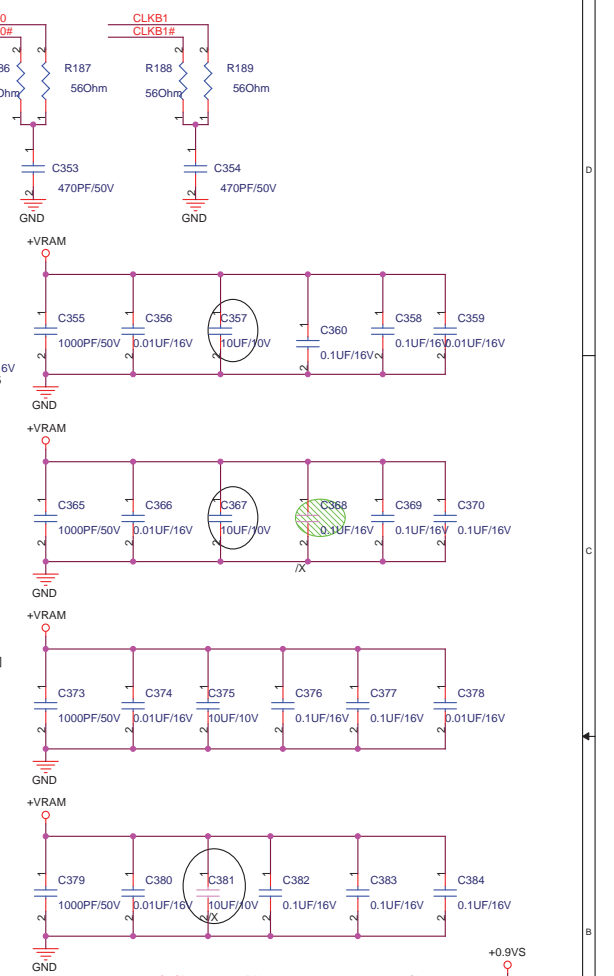
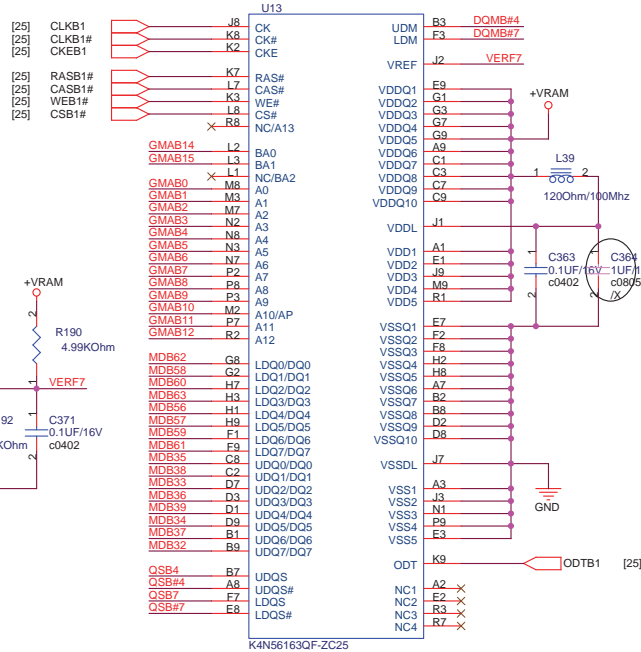
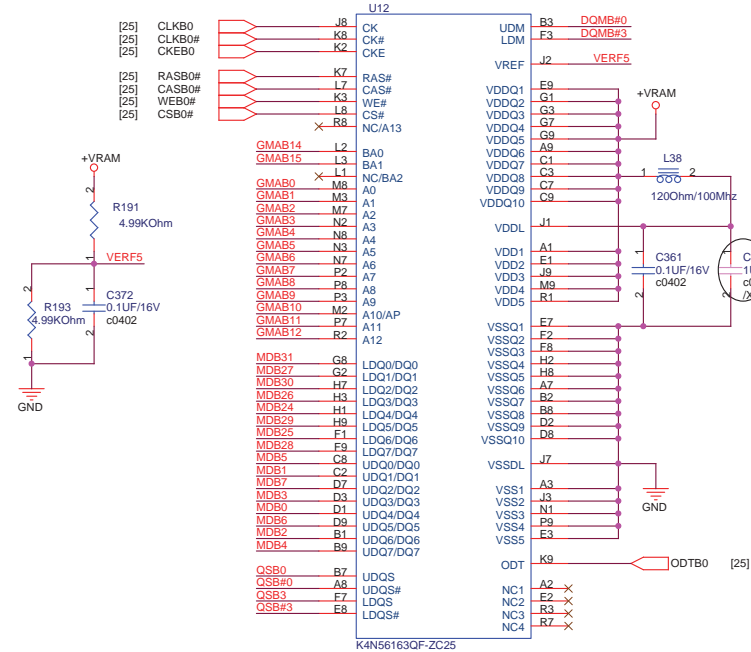


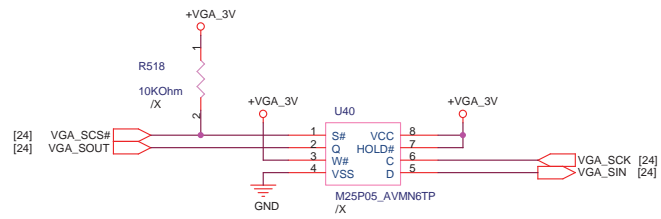






[25] GMAB[15..0]  
[25] QSB[7..0]  
[25] QSB#7..0  
[25] DQMB#7..0

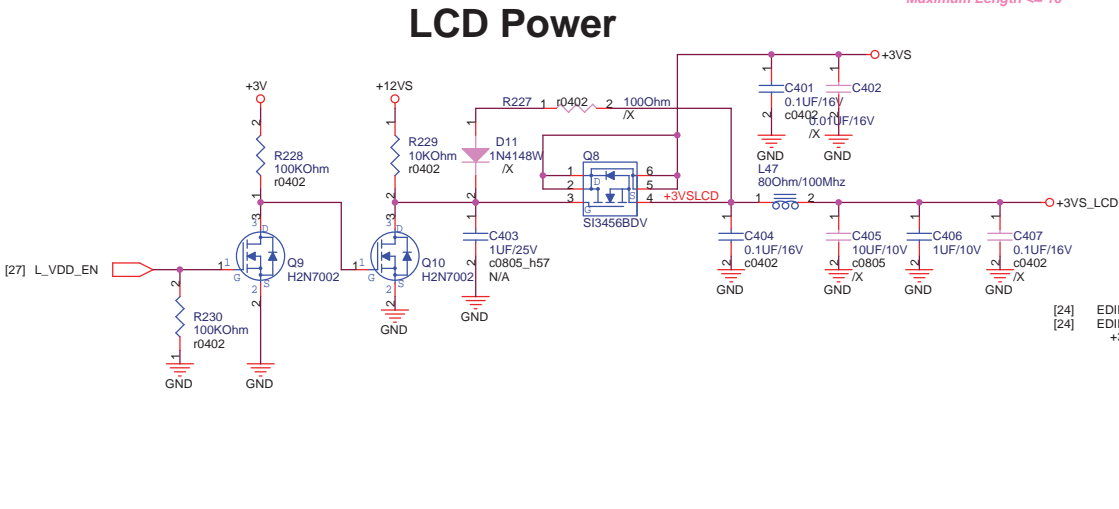




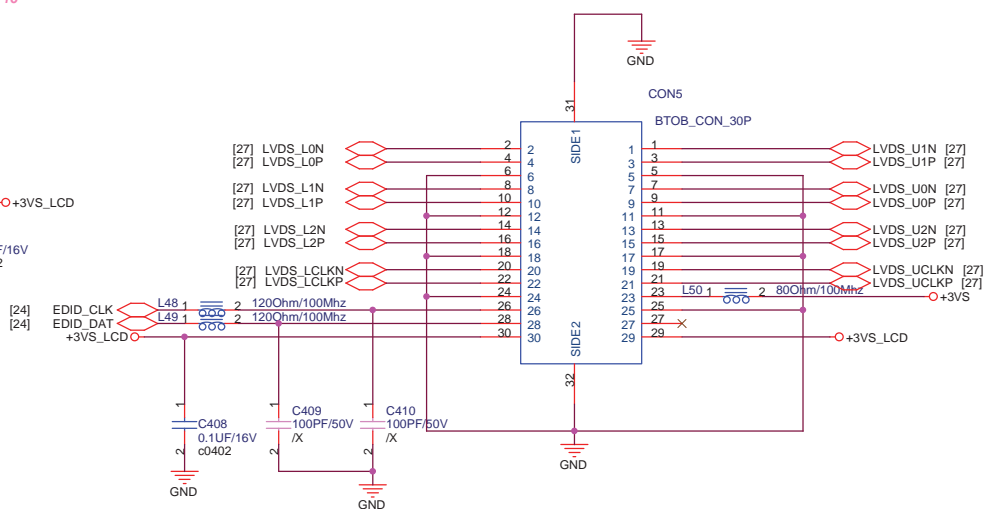




# LCD Backlight Control

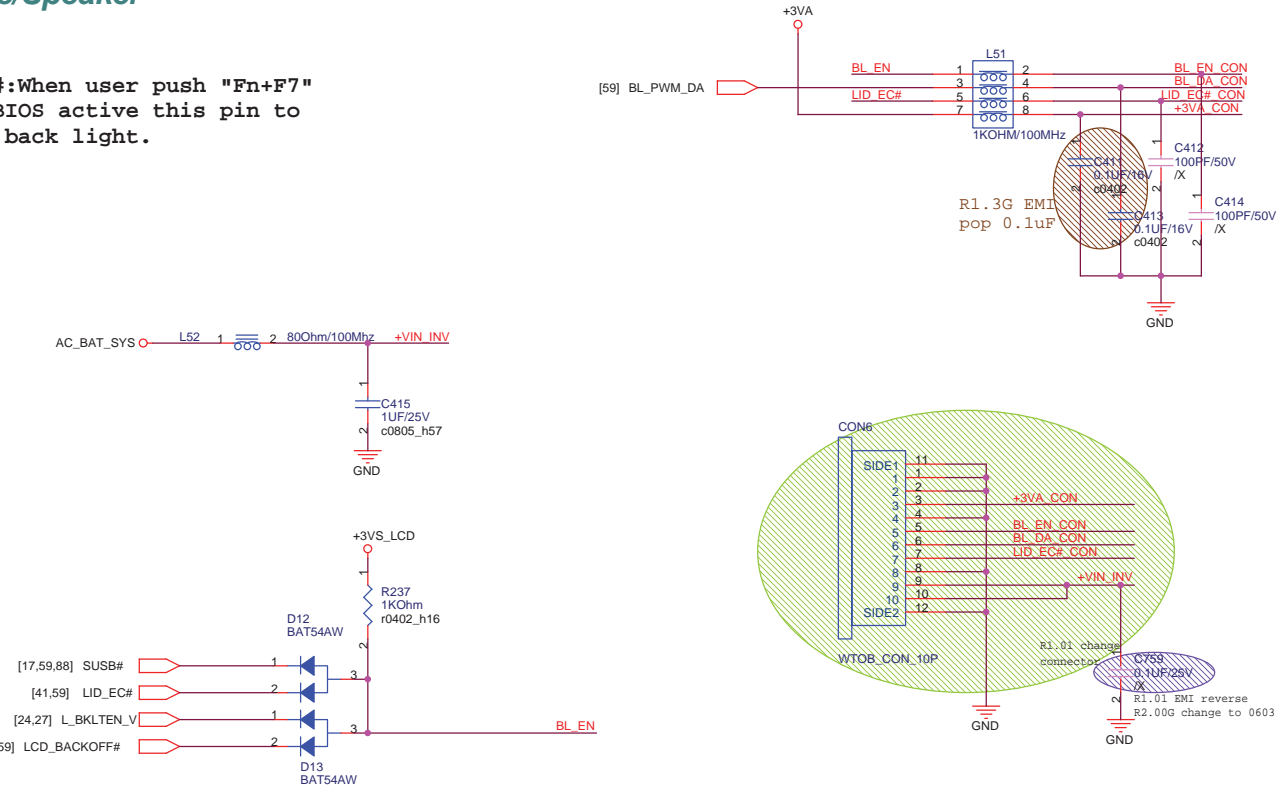


# LCD LVDS Interface



## INVERTER Interface/Speaker CONN.

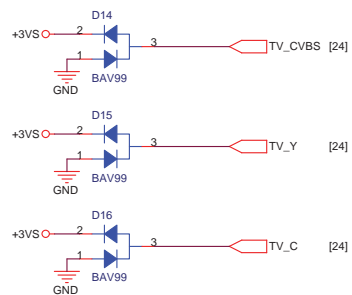
BIOS  
BACK\_OFF#:When user push "Fn+F7"  
button, BIOS active this pin to  
turn off back light.



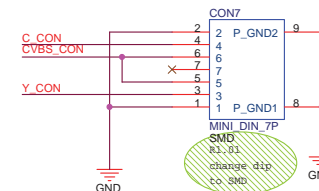
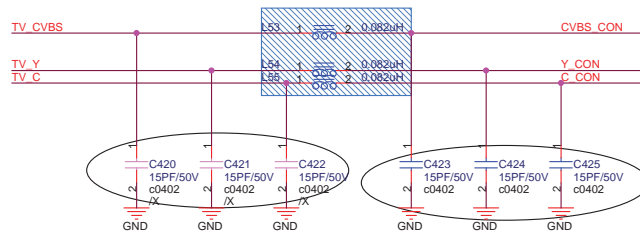
R1.01 remove R1 reserve pannel ID

ASUS		Title : LVDS & INVERTER	
ASUSTek COMPUTER INC		Engineer: Alan Chu	
Size	Project Name	Rev	
Custom	Z96Jm	1.0	
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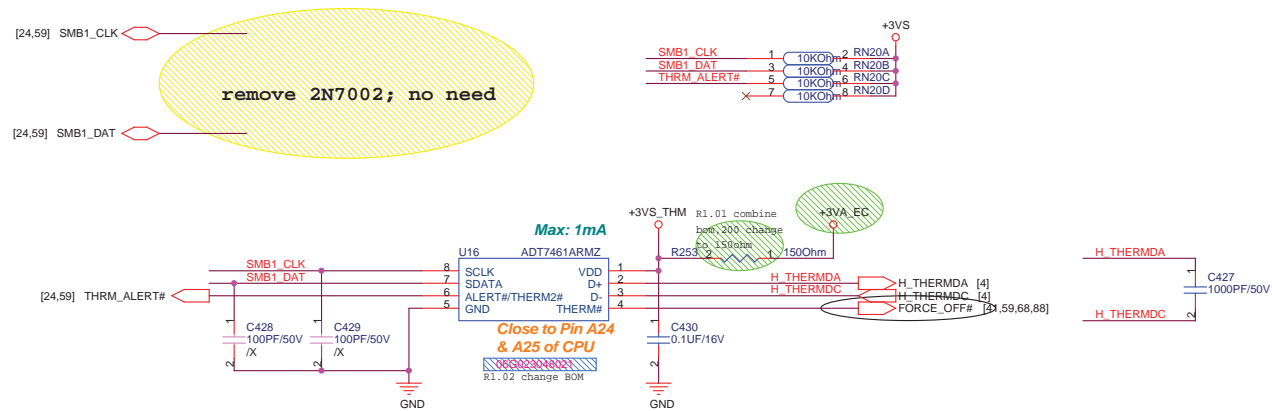
TV  
OUT



PLACE ESD  
Diodes near  
TV port



## Thermal Sensor



Route H\_THERMDA and H\_THERMDC on the same layer

-----OTHER SIGNALS

15 mils

-----GND

10 mils

-----H\_THERMDA(10 mils)

10 mils

-----H\_THERMDC(10 mils)

10 mils

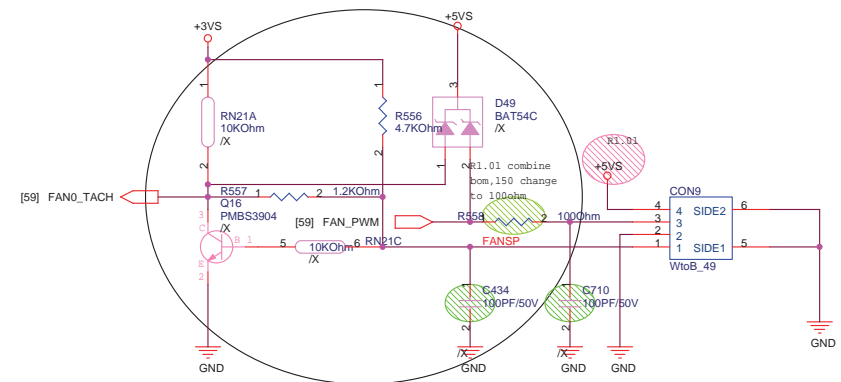
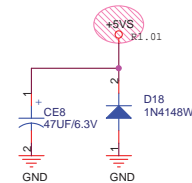
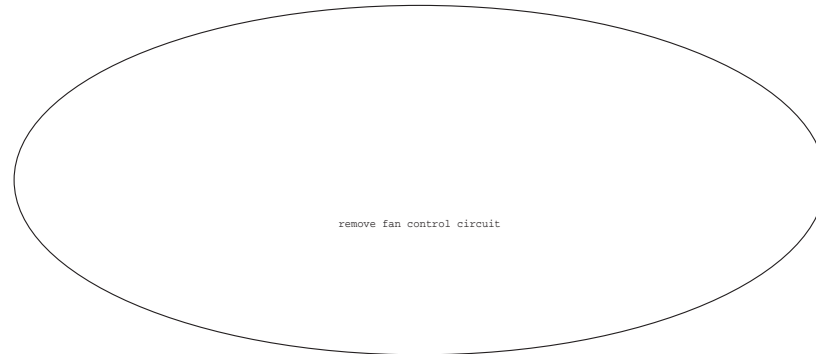
-----GND

15 mils

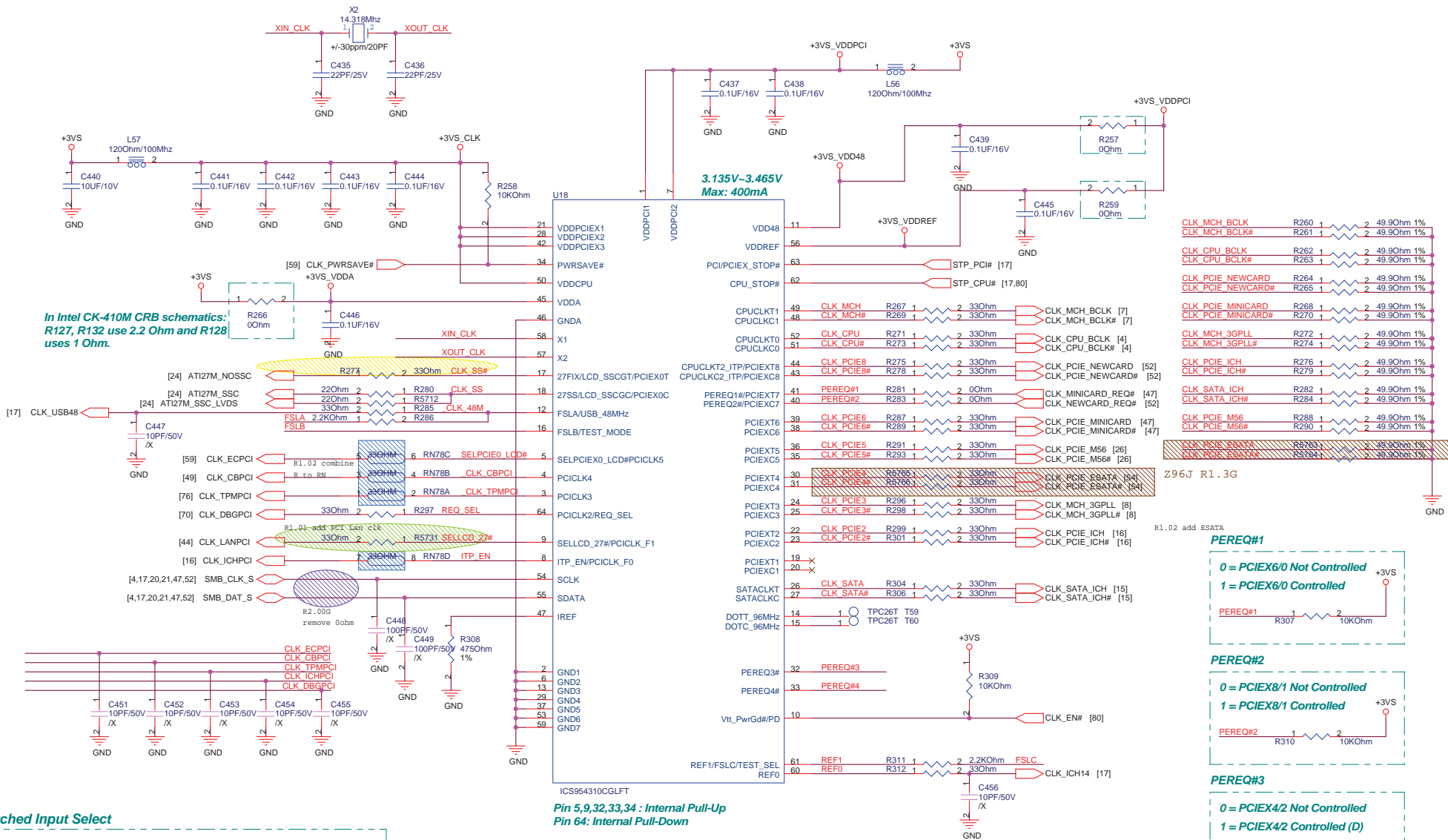
-----OTHER SIGNALS

Avoid FSB,Power

## DC FAN Control



CPU FAN will be forced on:  
1) Thermal Sensor Over-temperature  
2) WATCHDOG asserted by EC



In Intel CK-410M CRB schematics:  
R127, R132 use 2.2 Ohm and R128  
uses 1 Ohm.

3.135V~3.465V  
Max: 400mA

Z96J R1.3G

PEREQ#1

0 = PCIEX6/0 Not Controlled  
1 = PCIEX6/0 Controlled

PEREQ#2

0 = PCIEX8/1 Not Controlled  
1 = PCIEX8/1 Controlled

PEREQ#3

0 = PCIEX4/2 Not Controlled  
1 = PCIEX4/2 Controlled (D)

PEREQ#4

0 = PCIEX7/5/3 Not Controlled  
1 = PCIEX7/5/3 Controlled (D)

Latched Input Select

ITP\_EN/PCICLK\_F0

0 = SRC Pair  
1 = CPU\_IPT Pair

PCI\_CLK2/REQ\_SEL

0 = PCICLK(D)  
1 = PEREQ#

SELPCIE0\_LCD#/PCI\_CLK5

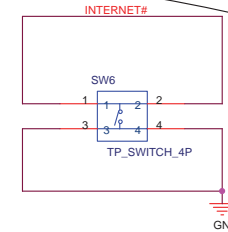
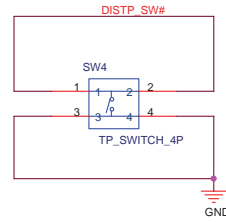
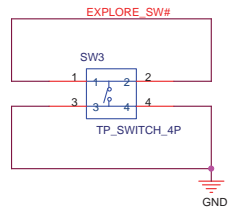
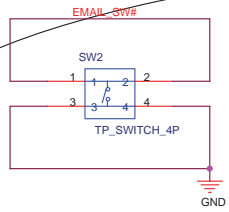
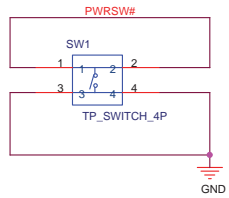
0 = LCD Clock (96MHz)  
1 = PCI Express (100MHz)

SELLCD\_27#/PCICLK\_F1

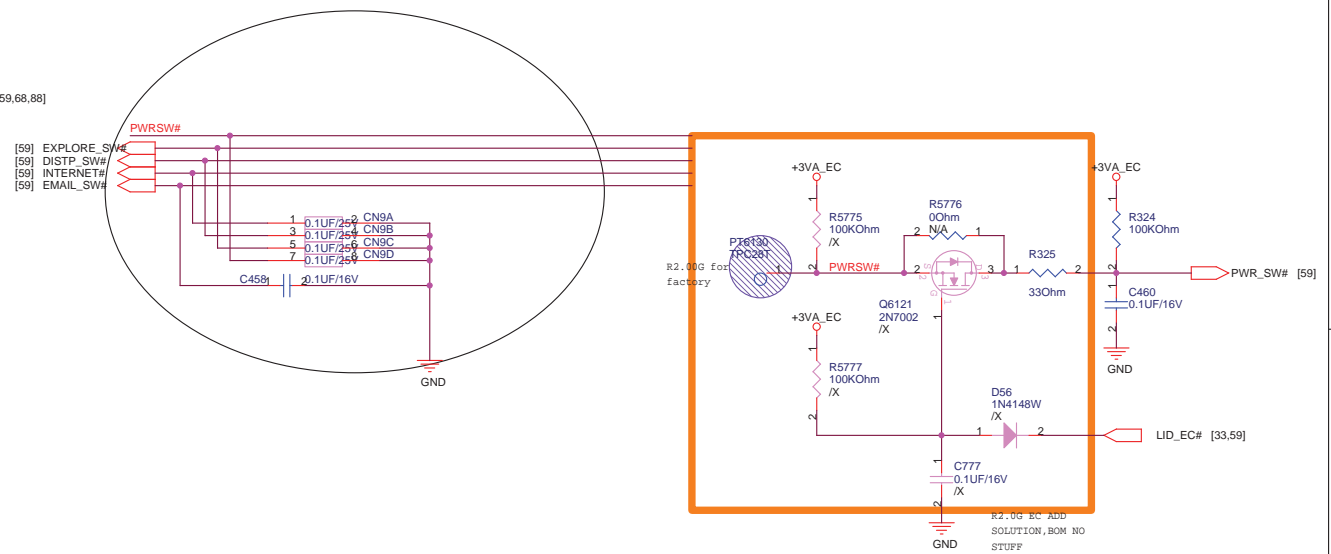
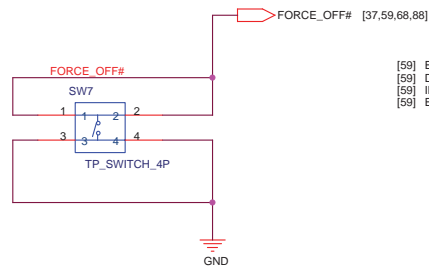
0 = 27MHzSS/27MHzSS# Pair  
1 = LCD\_CLK Pair

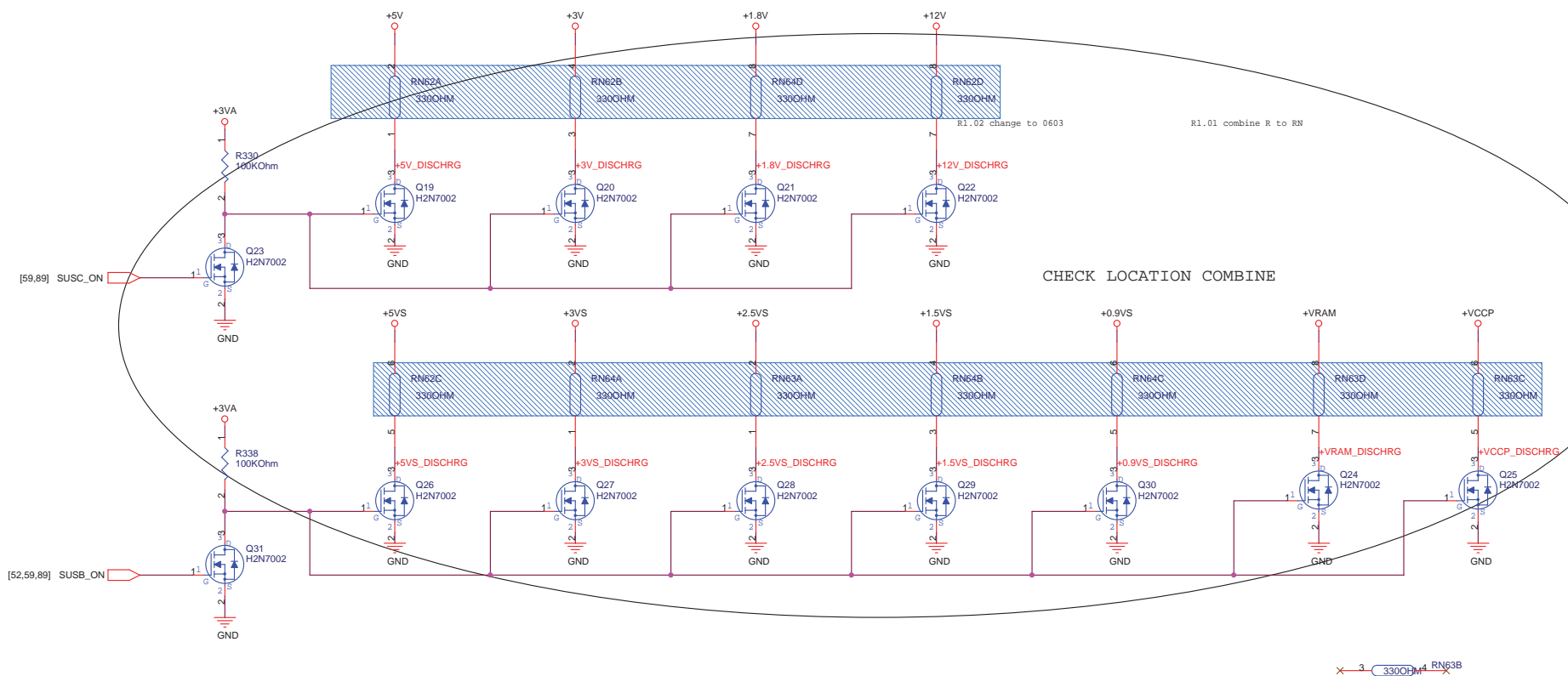
Reserved for Debug & Experiment

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

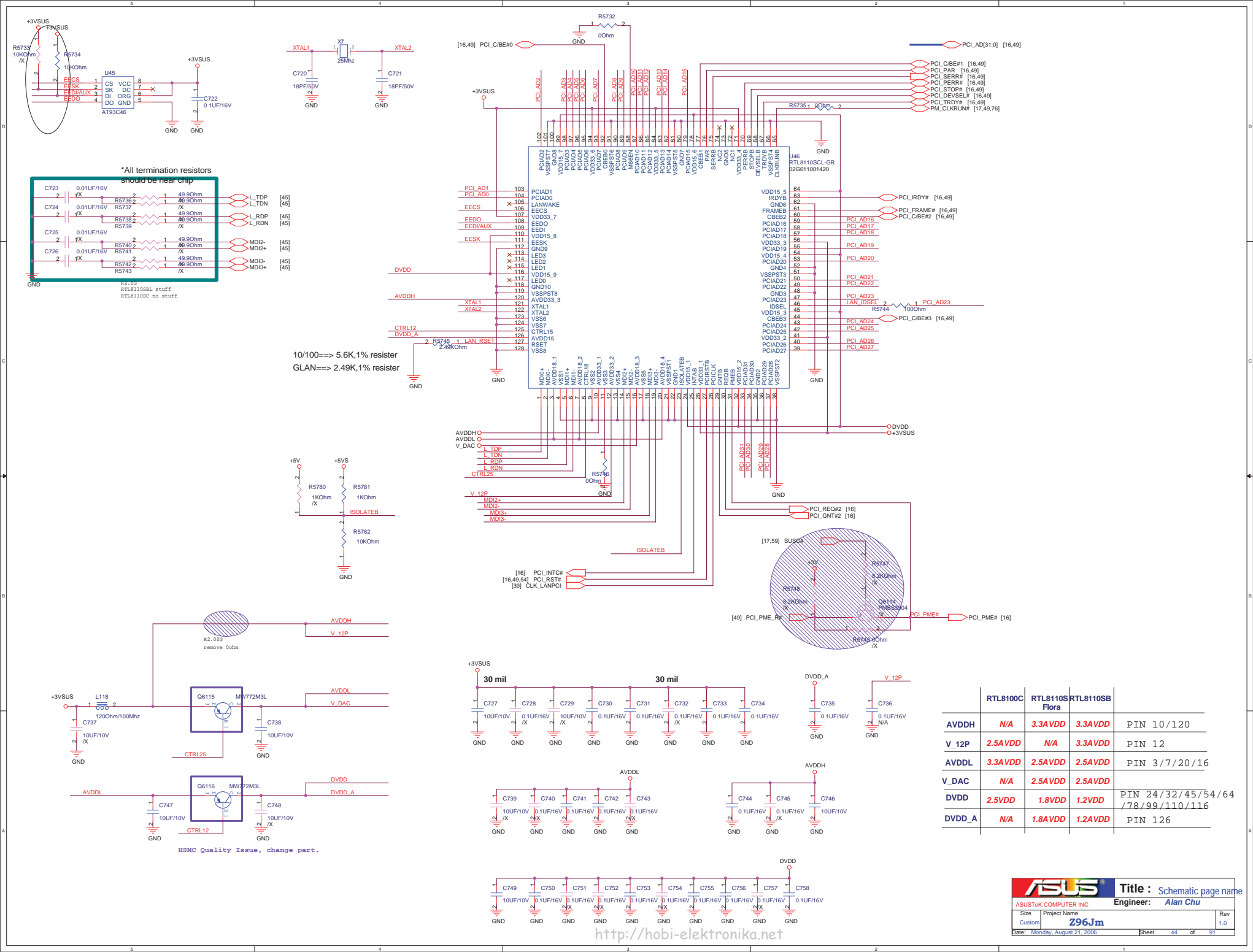


## SHUT\_DOWN#



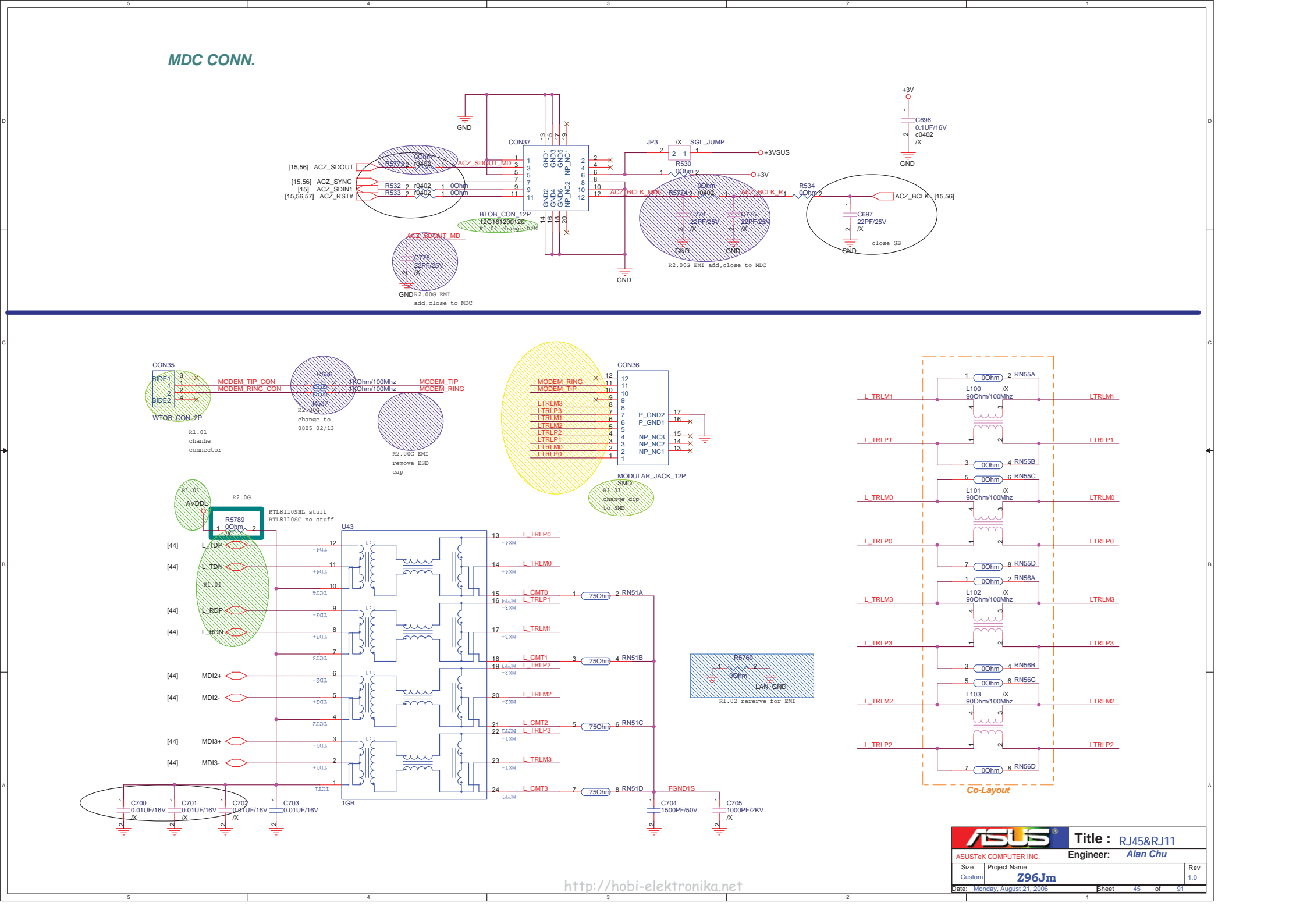
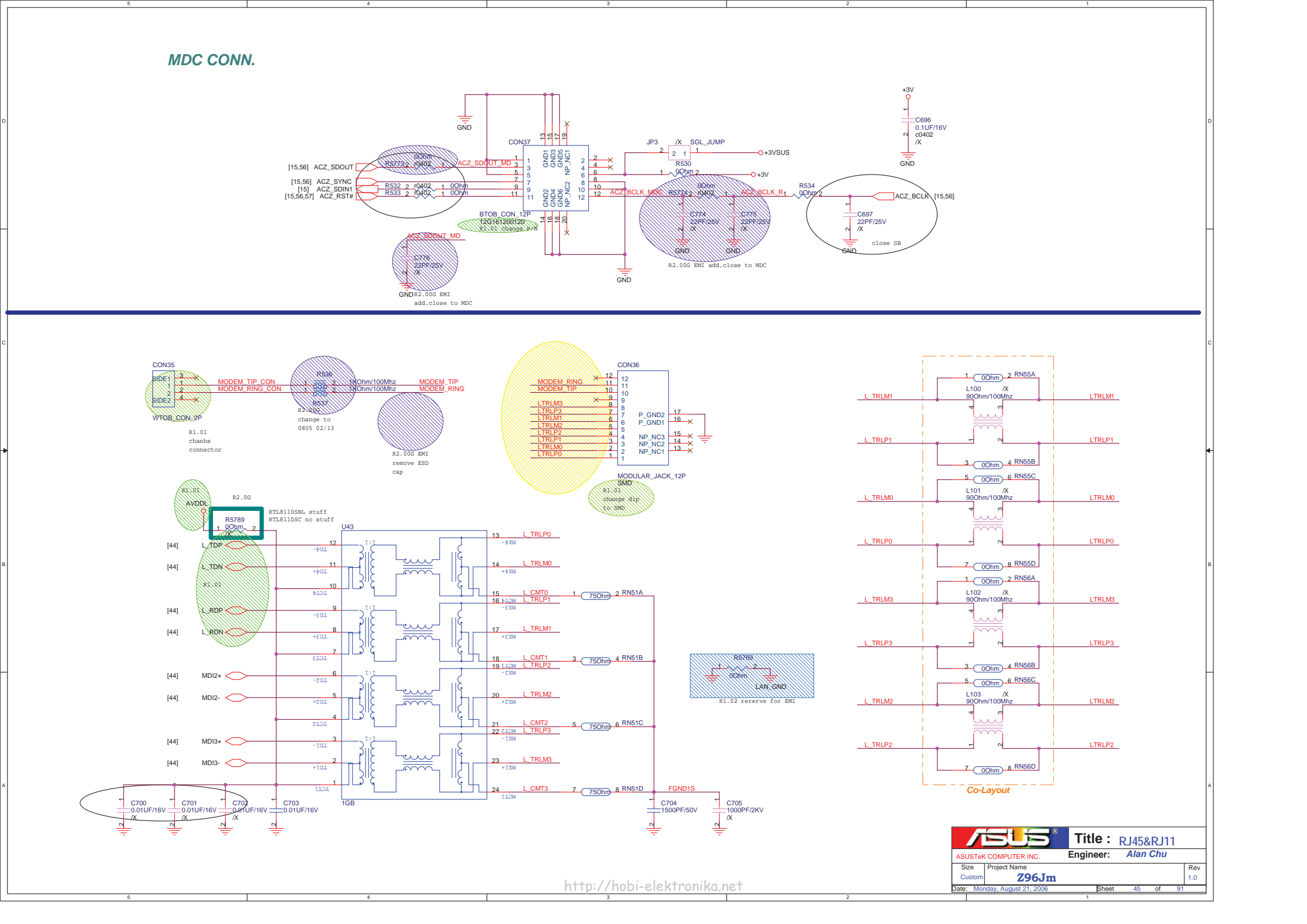


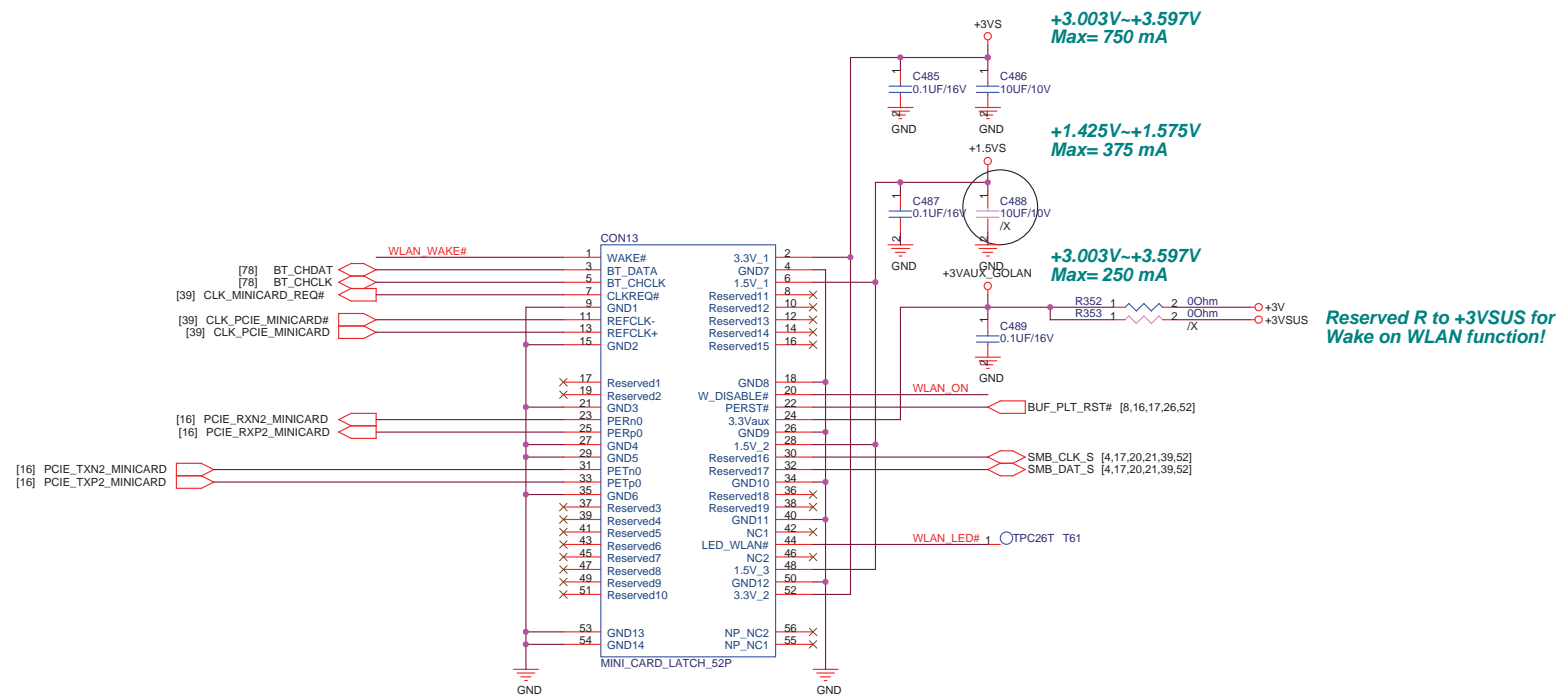




The image displays a detailed PCB layout for RJ45 and RJ11 ports. The layout is organized into several functional blocks:

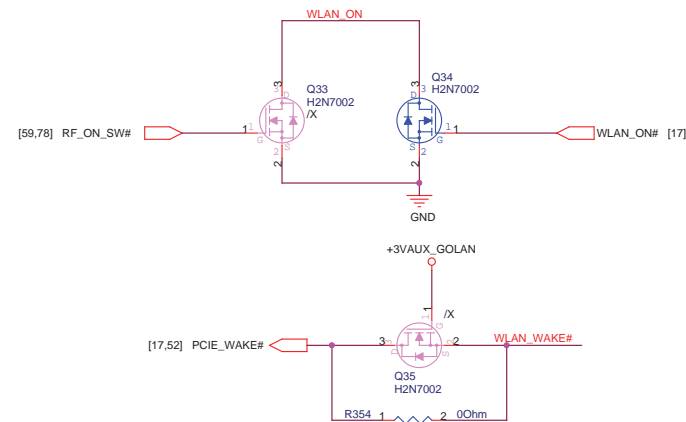
- MDC CONN. (Top):** This section shows the connection to the Modem Data Controller (MDC). It includes components like R577, R532, R533, R534, R574, R575, R576, R577, R578, R579, R580, R581, R582, R583, R584, R585, R586, R587, R588, R589, R590, R591, R592, R593, R594, R595, R596, R597, R598, R599, R600, R601, R602, R603, R604, R605, R606, R607, R608, R609, R610, R611, R612, R613, R614, R615, R616, R617, R618, R619, R620, R621, R622, R623, R624, R625, R626, R627, R628, R629, R630, R631, R632, R633, R634, R635, R636, R637, R638, R639, R640, R641, R642, R643, R644, R645, R646, R647, R648, R649, R650, R651, R652, R653, R654, R655, R656, R657, R658, R659, R660, R661, R662, R663, R664, R665, R666, R667, R668, R669, R670, R671, R672, R673, R674, R675, R676, R677, R678, R679, R680, R681, R682, R683, R684, R685, R686, R687, R688, R689, R690, R691, R692, R693, R694, R695, R696, R697, R698, R699, R700, R701, R702, R703, R704, R705, R706, R707, R708, R709, R710, R711, R712, R713, R714, R715, R716, R717, R718, R719, R720, R721, R722, R723, R724, R725, R726, R727, R728, R729, R730, R731, R732, R733, R734, R735, R736, R737, R738, R739, R740, R741, R742, R743, R744, R745, R746, R747, R748, R749, R750, R751, R752, R753, R754, R755, R756, R757, R758, R759, R760, R761, R762, R763, R764, R765, R766, R767, R768, R769, R770, R771, R772, R773, R774, R775, R776, R777, R778, R779, R780, R781, R782, R783, R784, R785, R786, R787, R788, R789, R790, R791, R792, R793, R794, R795, R796, R797, R798, R799, R800, R801, R802, R803, R804, R805, R806, R807, R808, R809, R810, R811, R812, R813, R814, R815, R816, R817, R818, R819, R820, R821, R822, R823, R824, R825, R826, R827, R828, R829, R830, R831, R832, R833, R834, R835, R836, R837, R838, R839, R840, R841, R842, R843, R844, R845, R846, R847, R848, R849, R850, R851, R852, R853, R854, R855, R856, R857, R858, R859, R860, R861, R862, R863, R864, R865, R866, R867, R868, R869, R870, R871, R872, R873, R874, R875, R876, R877, R878, R879, R880, R881, R882, R883, R884, R885, R886, R887, R888, R889, R890, R891, R892, R893, R894, R895, R896, R897, R898, R899, R900, R901, R902, R903, R904, R905, R906, R907, R908, R909, R910, R911, R912, R913, R914, R915, R916, R917, R918, R919, R920, R921, R922, R923, R924, R925, R926, R927, R928, R929, R930, R931, R932, R933, R934, R935, R936, R937, R938, R939, R940, R941, R942, R943, R944, R945, R946, R947, R948, R949, R950, R951, R952, R953, R954, R955, R956, R957, R958, R959, R960, R961, R962, R963, R964, R965, R966, R967, R968, R969, R970, R971, R972, R973, R974, R975, R976, R977, R978, R979, R980, R981, R982, R983, R984, R985, R986, R987, R988, R989, R990, R991, R992, R993, R994, R995, R996, R997, R998, R999, R1000, R1001, R1002, R1003, R1004, R1005, R1006, R1007, R1008, R1009, R1010, R1011, R1012, R1013, R1014, R1015, R1016, R1017, R1018, R1019, R1020, R1021, R1022, R1023, R1024, R1025, R1026, R1027, R1028, R1029, R1030, R1031, R1032, R1033, R1034, R1035, R1036, R1037, R1038, R1039, R1040, R1041, R1042, R1043, R1044, R1045, R1046, R1047, R1048, R1049, R1050, R1051, R1052, R1053, R1054, R1055, R1056, R1057, R1058, R1059, R1060, R1061, R1062, R1063, R1064, R1065, R1066, R1067, R1068, R1069, R1070, R1071, R1072, R1073, R1074, R1075, R1076, R1077, R1078, R1079, R1080, R1081, R1082, R1083, R1084, R1085, R1086, R1087, R1088, R1089, R1090, R1091, R1092, R1093, R1094, R1095, R1096, R1097, R1098, R1099, R1100, R1101, R1102, R1103, R1104, R1105, R1106, R1107, R1108, R1109, R1110, R1111, R1112, R1113, R1114, R1115, R1116, R1117, R1118, R1119, R1120, R1121, R1122, R1123, R1124, R1125, R1126, R1127, R1128, R1129, R1130, R1131, R1132, R1133, R1134, R1135, R1136, R1137, R1138, R1139, R1140, R1141, R1142, R1143, R1144, R1145, R1146, R1147, R1148, R1149, R1150, R1151, R1152, R1153, R1154, R1155, R1156, R1157, R1158, R1159, R1160, R1161, R1162, R1163, R1164, R1165, R1166, R1167, R1168, R1169, R1170, R1171, R1172, R1173, R1174, R1175, R1176, R1177, R1178, R1179, R1180, R1181, R1182, R1183, R1184, R1185, R1186, R1187, R1188, R1189, R1190, R1191, R1192, R1193, R1194, R1195, R1196, R1197, R1198, R1199, R1200, R1201, R1202, R1203, R1204, R1205, R1206, R1207, R1208, R1209, R1210, R1211, R1212, R1213, R1214, R1215, R1216, R1217, R1218, R1219, R1220, R1221, R1222, R1223, R1224, R1225, R1226, R1227, R1228, R1229, R1230, R1231, R1232, R1233, R1234, R1235, R1236, R1237, R1238, R1239, R1240, R1241, R1242, R1243, R1244, R1245, R1246, R1247, R1248, R1249, R1250, R1251, R1252, R1253, R1254, R1255, R1256, R1257, R1258, R1259, R1260, R1261, R1262, R1263, R1264, R1265, R1266, R1267, R1268, R1269, R1270, R1271, R1272, R1273, R1274, R1275, R1276, R1277, R1278, R1279, R1280, R1281, R1282, R1283, R1284, R1285, R1286, R1287, R1288, R1289, R1290, R1291, R1292, R1293, R1294, R1295, R1296, R1297, R1298, R1299, R1300, R1301, R1302, R1303, R1304, R1305, R1306, R1307, R1





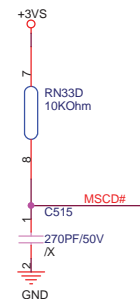
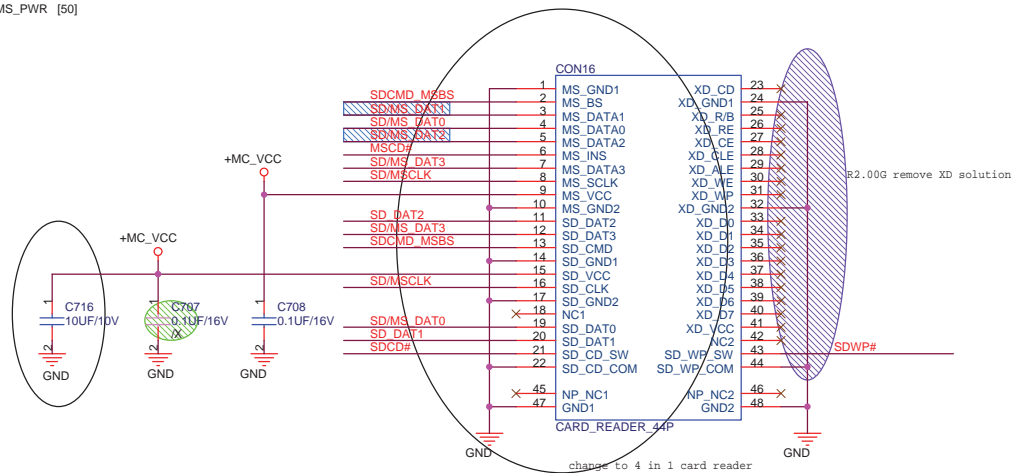
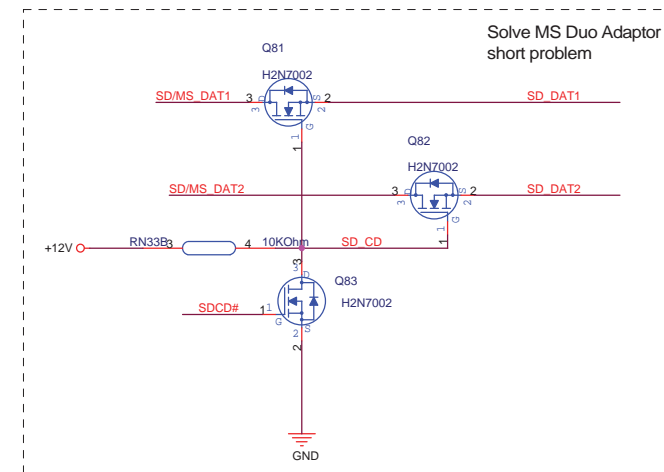
**H54 & H56**

R1\_01 remove  
connector, change to  
screw

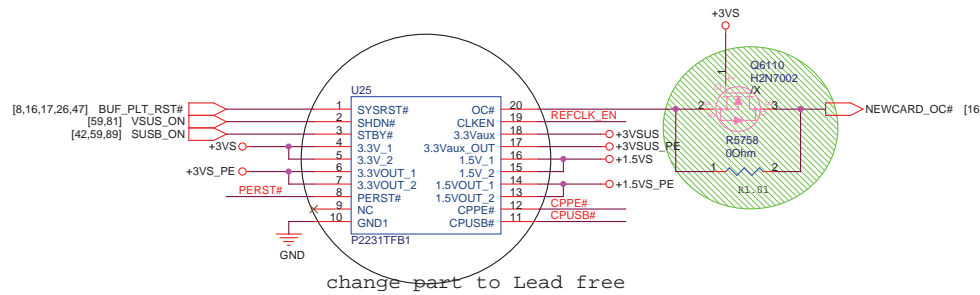
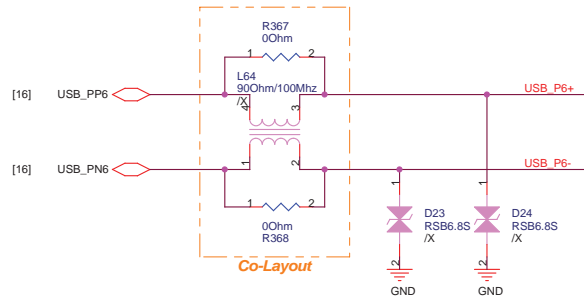




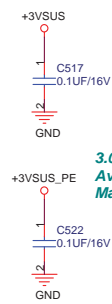
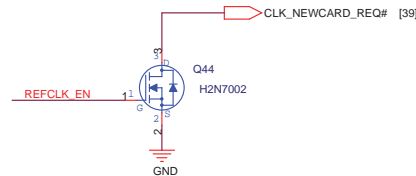




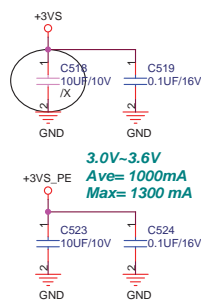




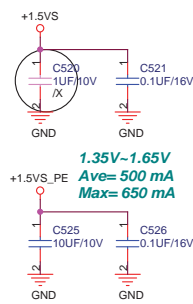
change part to Lead free



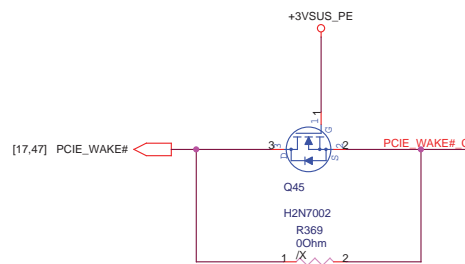
3.0V~3.6V  
Ave= 200mA  
Max= 275 mA



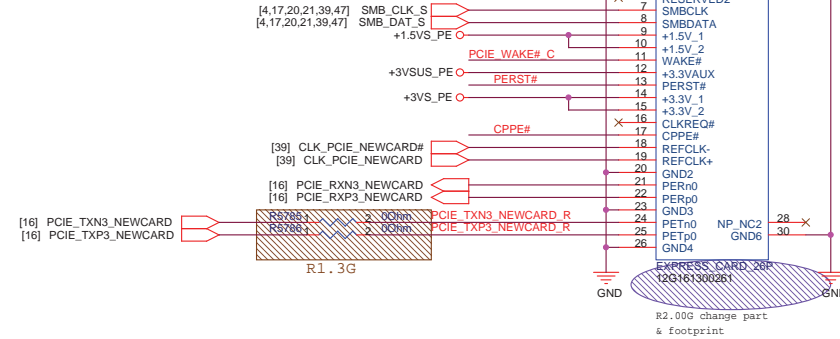
3.0V~3.6V  
Ave= 1000mA  
Max= 1300 mA



1.35V~1.65V  
Ave= 500 mA  
Max= 650 mA

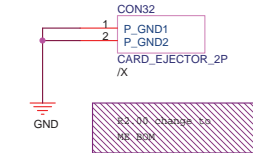


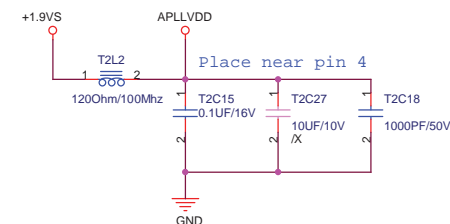
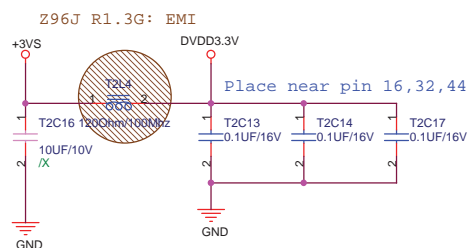
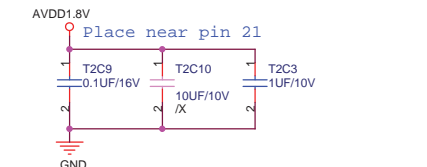
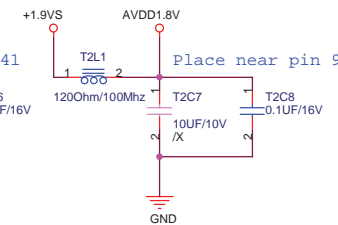
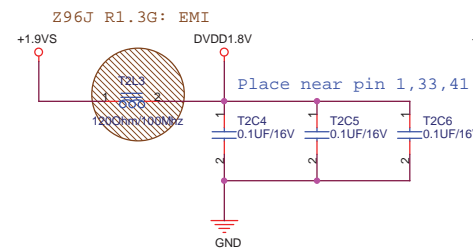
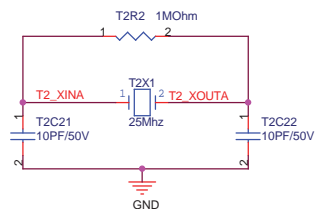
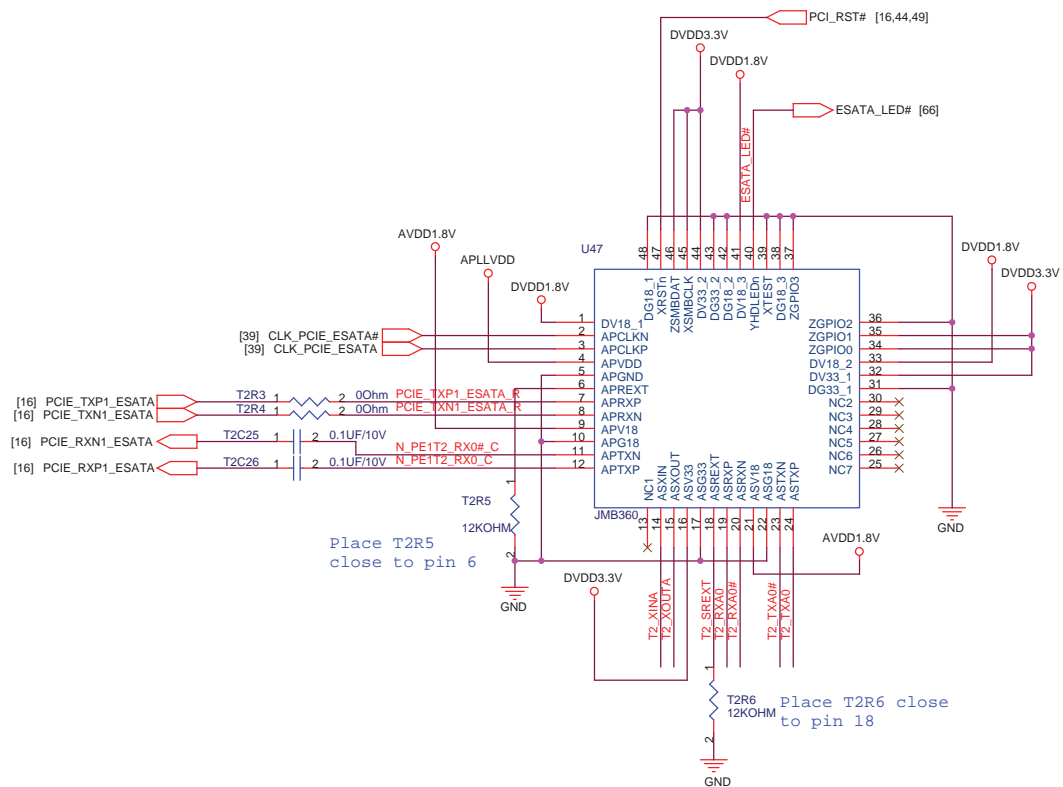
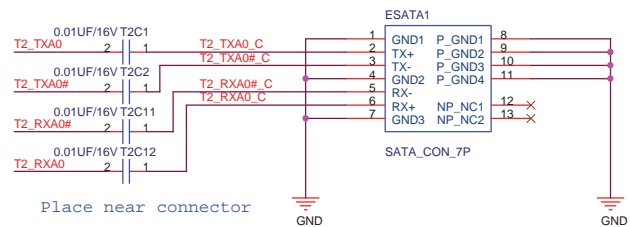
!! ExpressCard Standard 1.0:  
Change Pin7 from RESERVED to SMBCLK  
Change Pin8 from SMBCLK to SMBDATA  
Change Pin9 from SMBDATA to +1.5V



NewCard Header

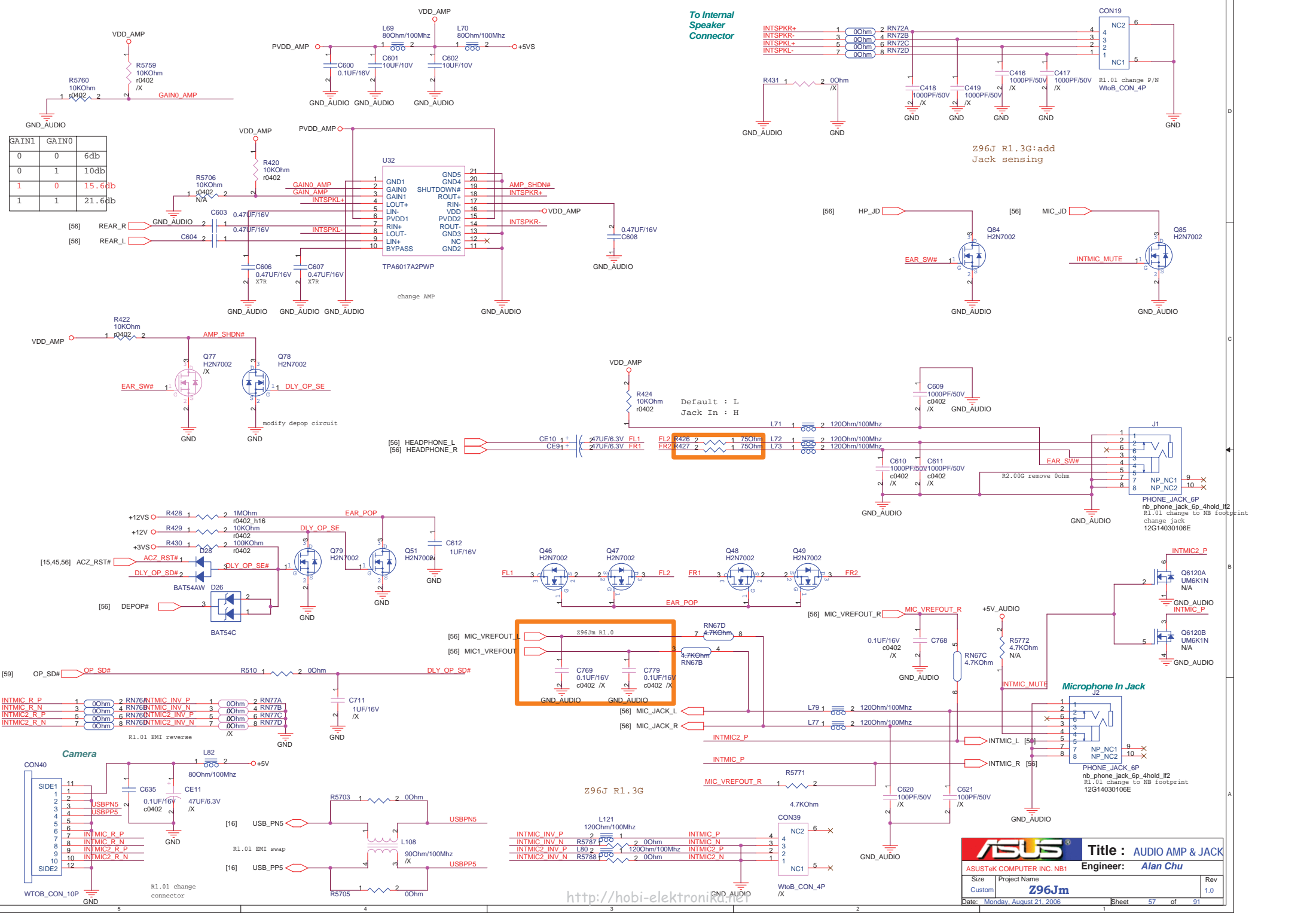
NewCard Ejector





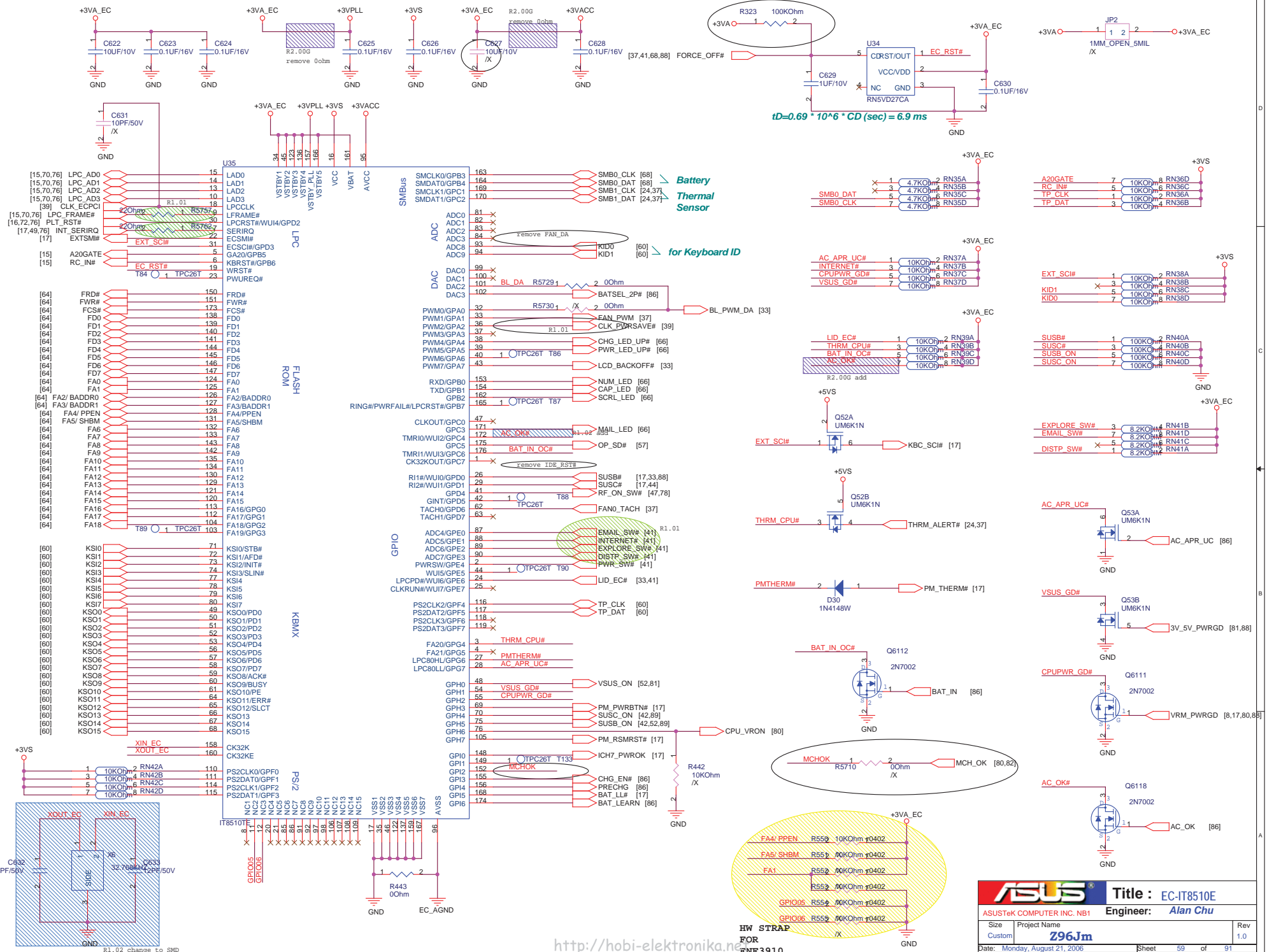
<b>ASUS</b>		<b>Title : ESATA JMB360</b>	
ASUSTek COMPUTER INC		Engineer: Alan Chu	
Size A3	Project Name <b>Z96Jm</b>	Rev 1.0	
Date: Monday, August 21, 2006		Sheet 54	of 91





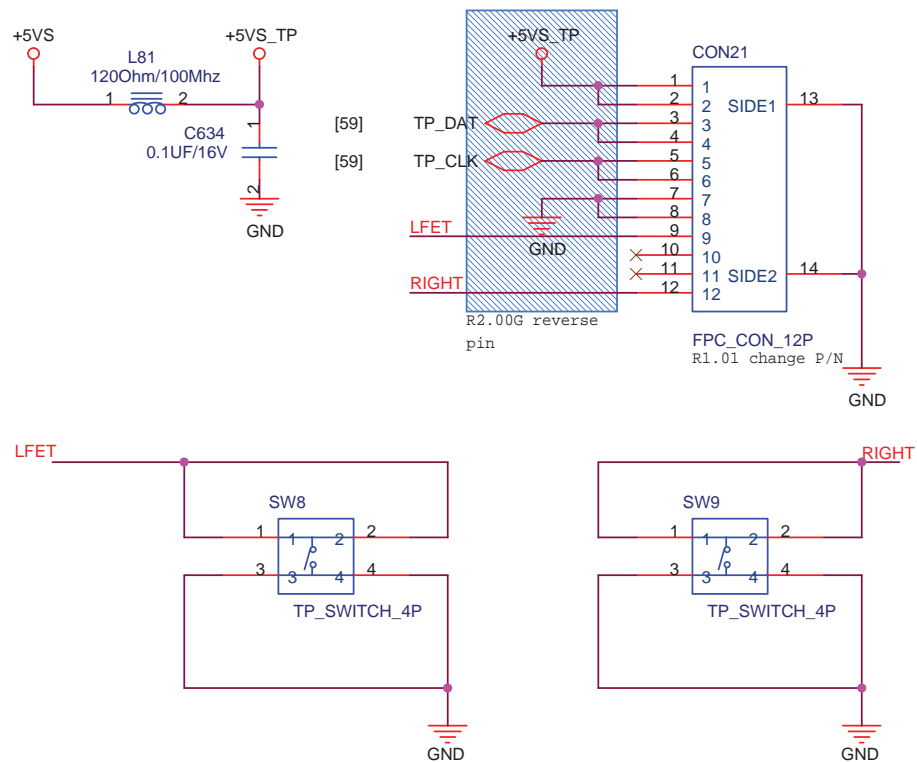
GAIN1	GAIN0	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db

INTMIC_R_P	1	00hm	2	RN76	INTMIC_INV_P	1	00hm	2	RN77A
INTMIC_R_N	3	00hm	4	RN76B	INTMIC_INV_N	3	00hm	4	RN77B
INTMIC2_R_P	5	00hm	6	RN76C	INTMIC2_INV_P	5	00hm	6	RN77C
INTMIC2_R_N	7	00hm	8	RN76D	INTMIC2_INV_N	7	00hm	8	RN77D

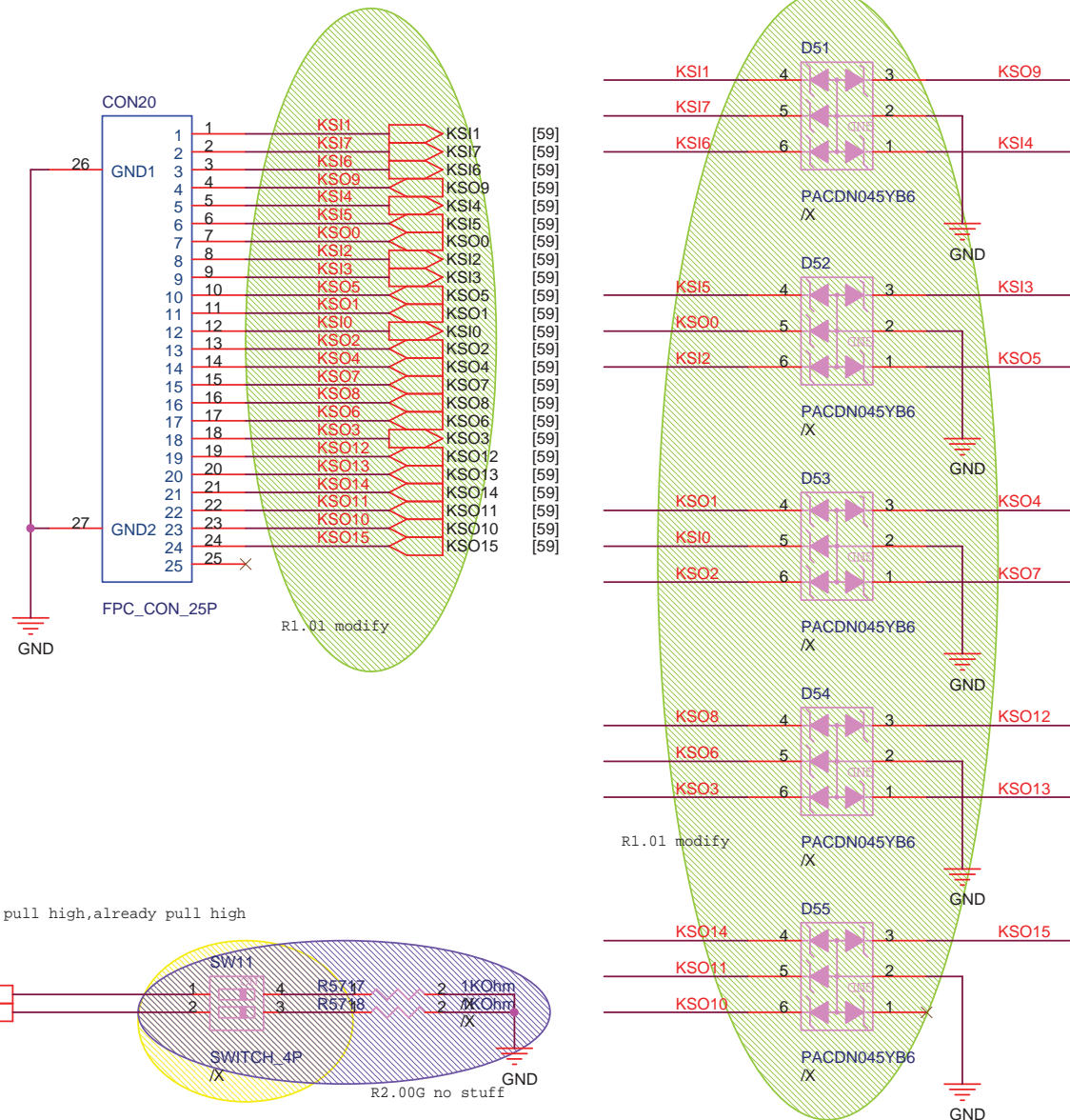


http://hobi-elektronika.net

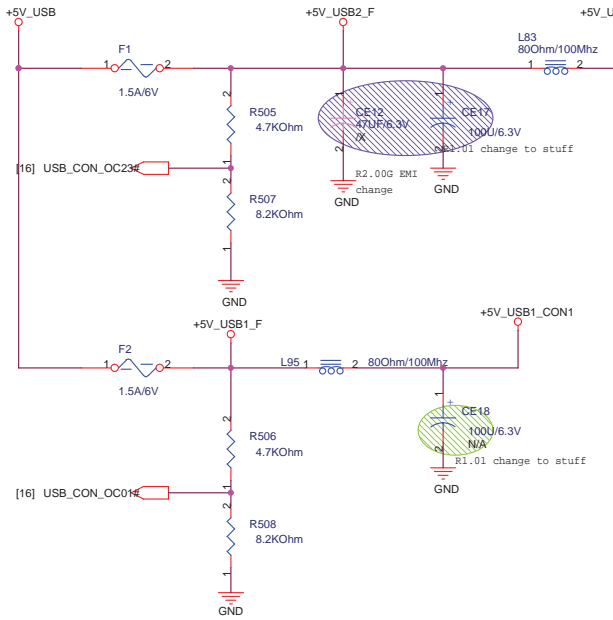
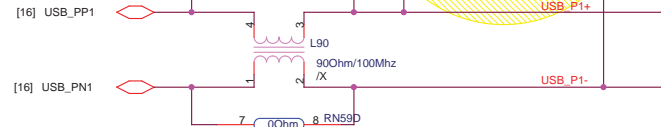
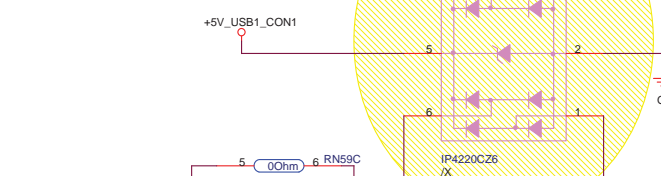
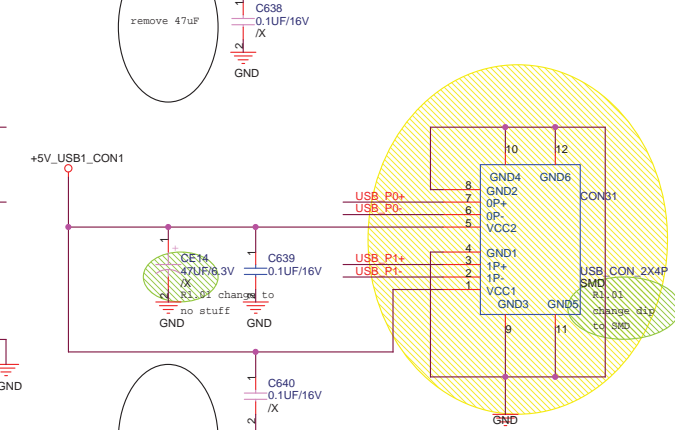
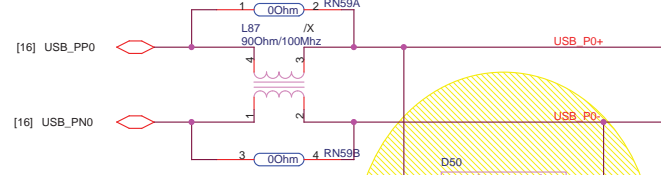
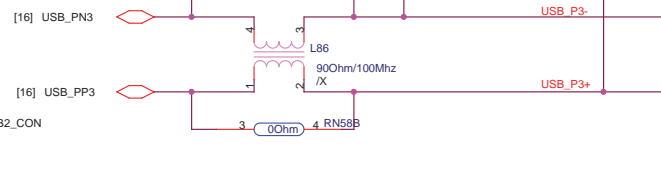
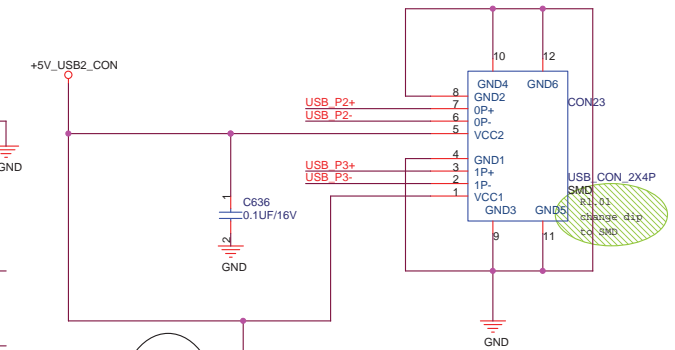
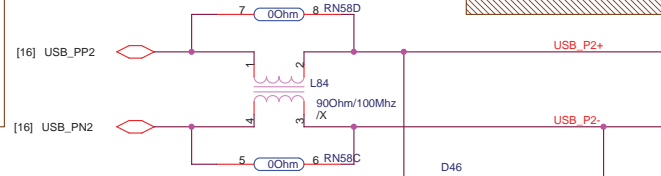
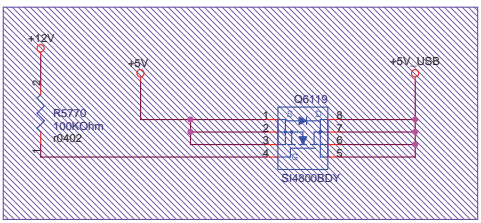
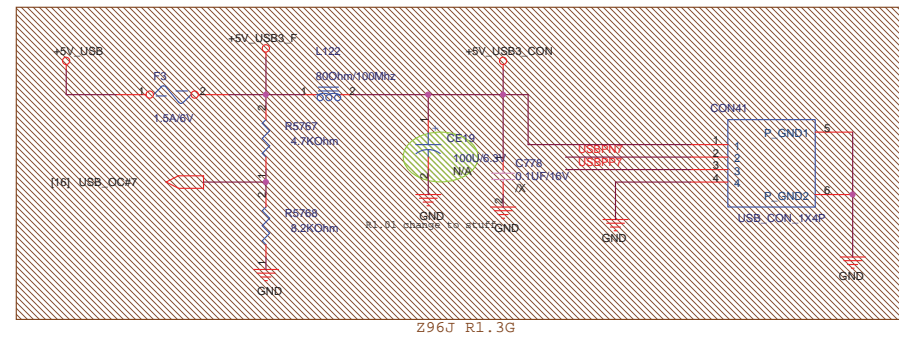
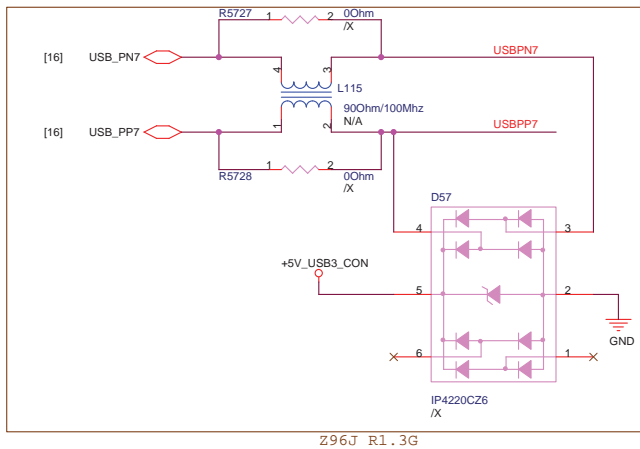
## For Touch-Pad



## For Keyboard





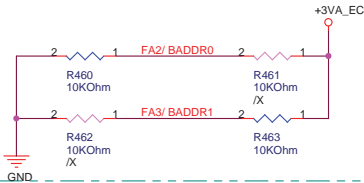


ISA ROM

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

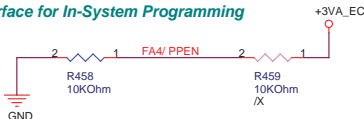
00: PNPCNG Access Register Pair Are 002Eh and 002Fh  
10: PNPCNG Access Register Pair Are 004Eh and 004Fh  
01: PNPCNG Access Register Pair Are Determined by  
EC Domain Registers SWCBALR and SWCBAHR.  
11: Reserved



Note: Sampled at VSTBY Power Up Reset

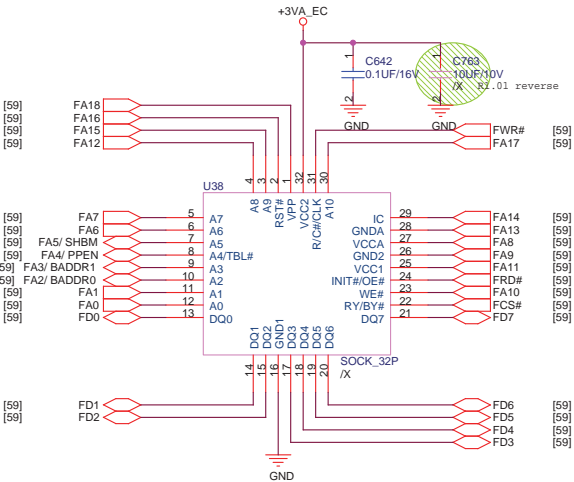
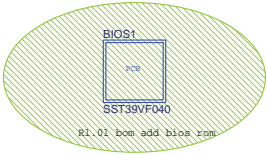
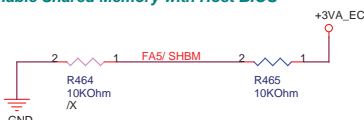
FA4/ PPEN

0: Normal  
1: KBS Interface Pins Are Switched to Parallel Port  
Interface for In-System Programming



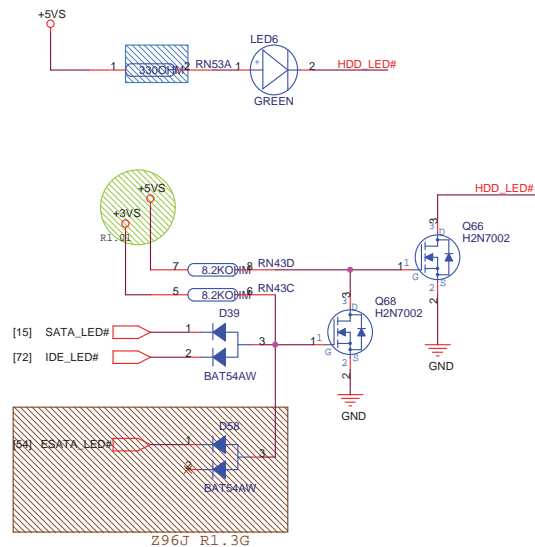
FA5/ SHBM

0: Disable Shared Memory with Host BIOS  
1: Enable Shared Memory with Host BIOS

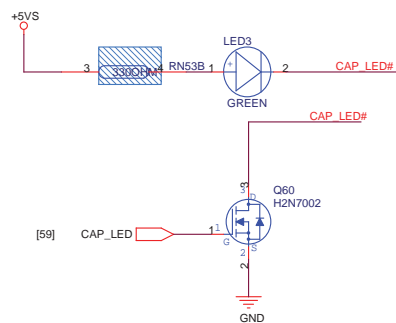


**For LED**

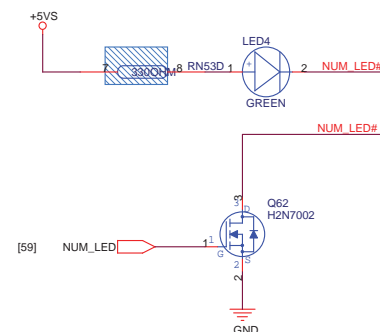
**For SATA/IDE LED**



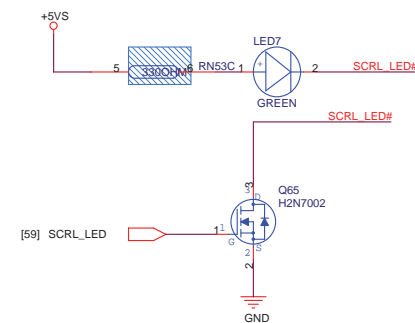
**for Cap. Lock**



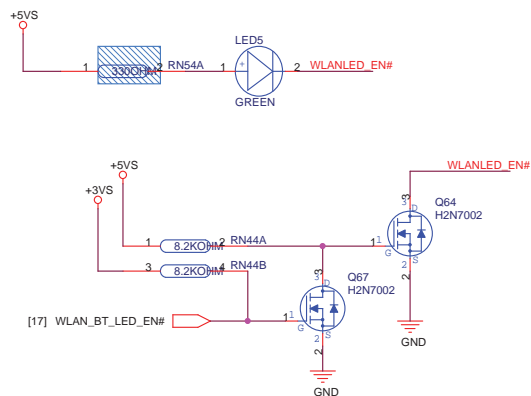
**for Num Lock**



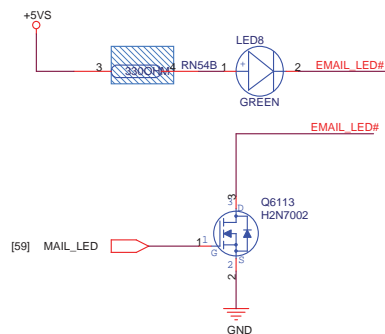
### for Scroll Lock



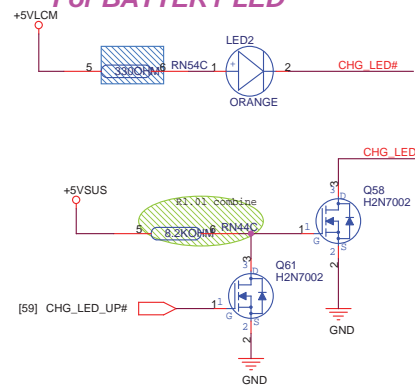
**For WireLess LED**



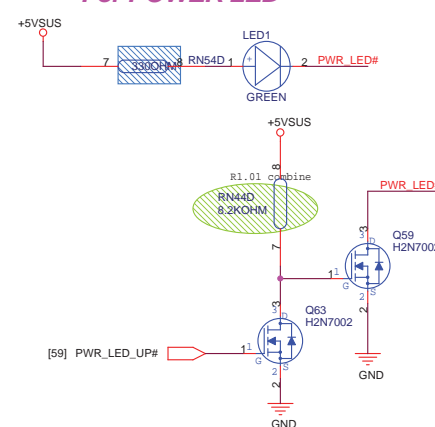
**for email**



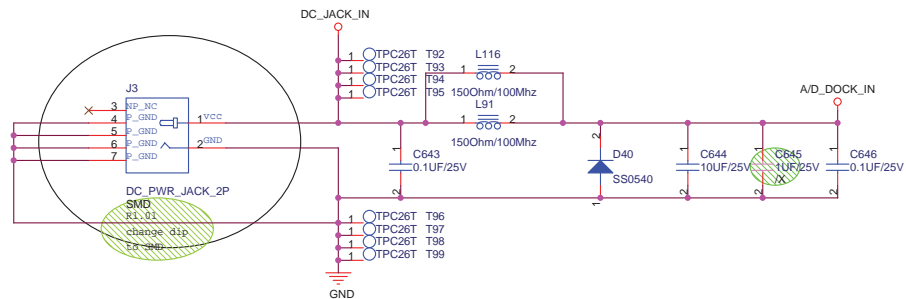
**For BATTERY LED**



**For POWER LED**

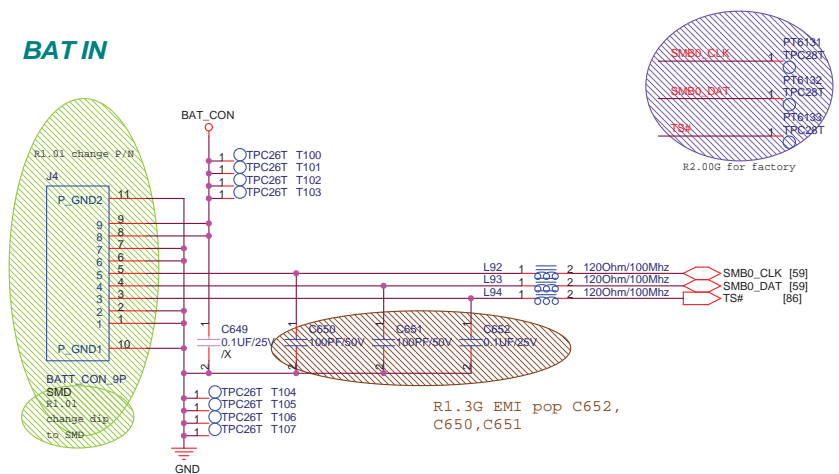


## DC IN

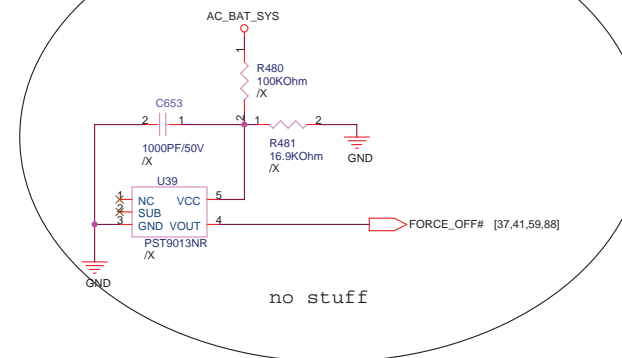


remove AC DC detect; no need

## BAT IN

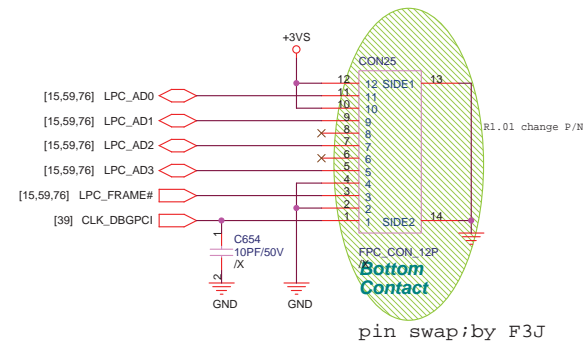


## Without Battery & Pull out Adapter

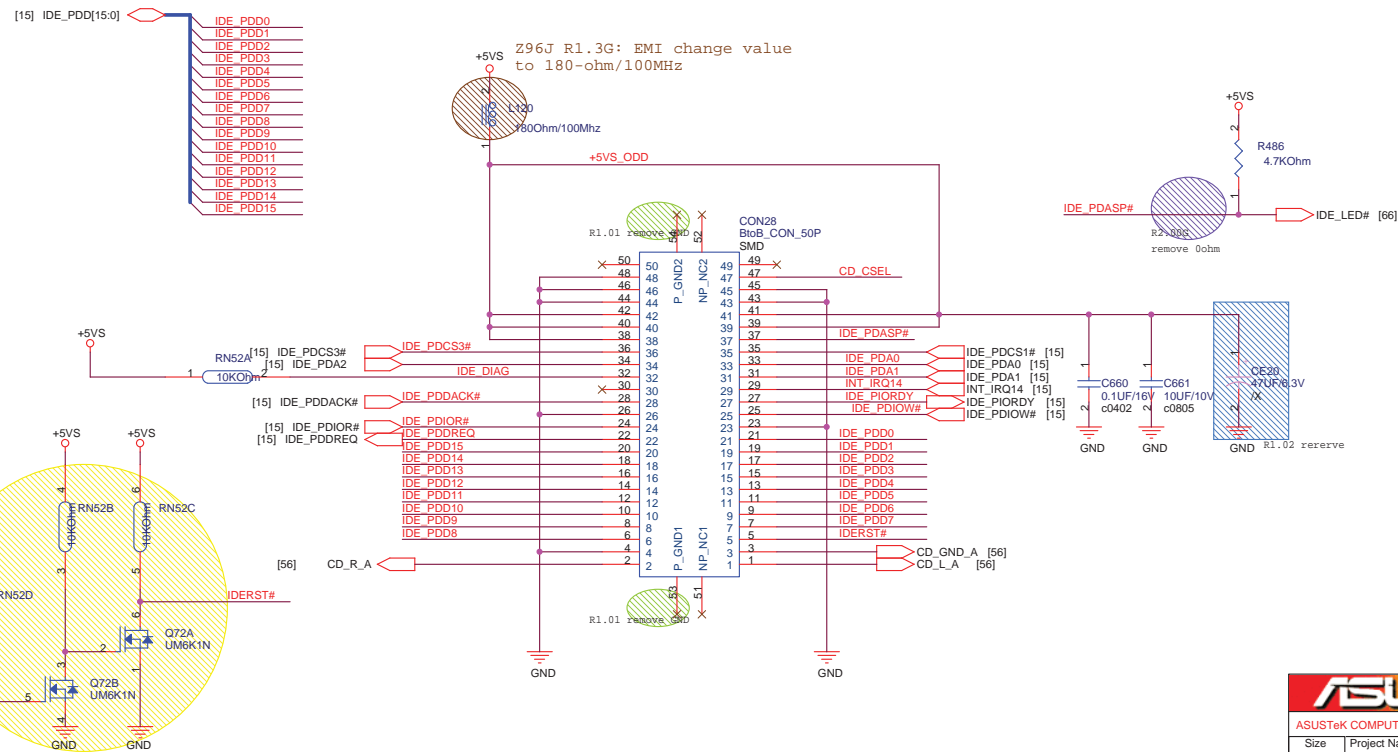


no stuff

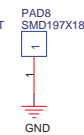
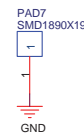
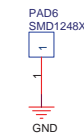
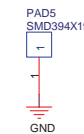
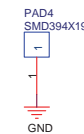
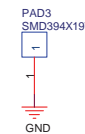
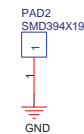
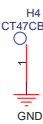
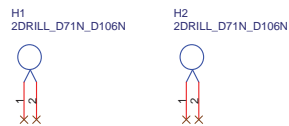
*For Debug*



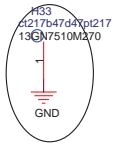
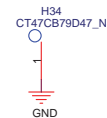
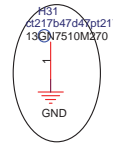
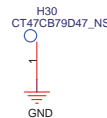
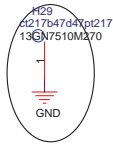
**ODD**



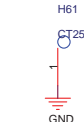
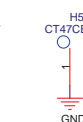
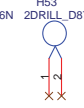
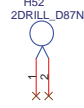
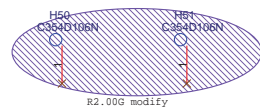
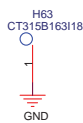
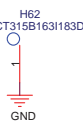
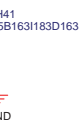
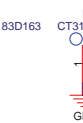
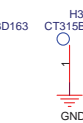
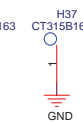
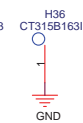
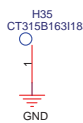




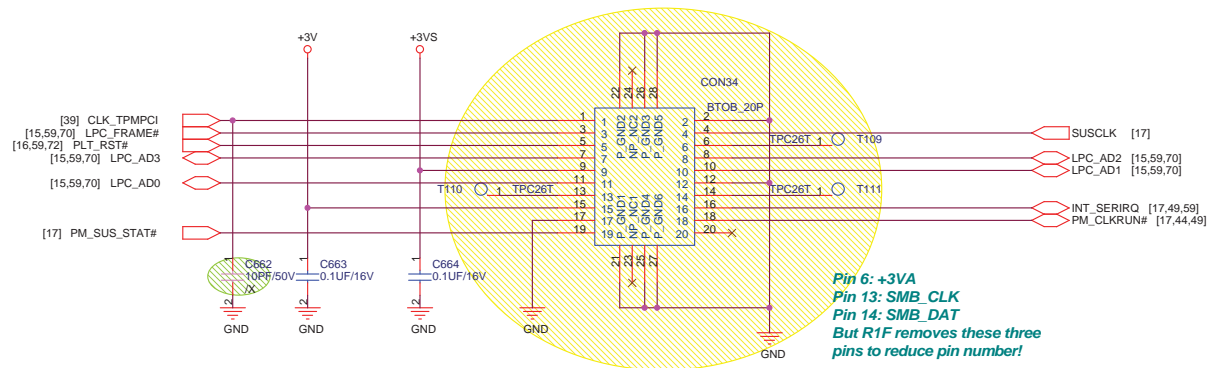
### FOR SCREW HOLE



### FOR SCREW HOLE



## For TPM Module



**For Bluetooth**

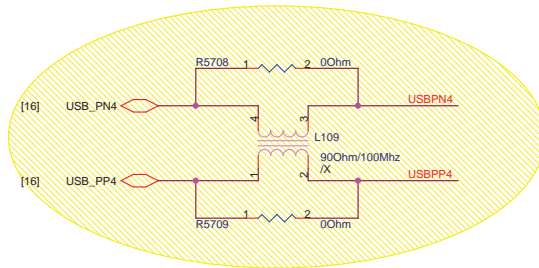
The diagram illustrates the electrical connections for a Bluetooth module. It is divided into two main sections: the module's external interface and its internal power/switching circuitry.

**Module External Interface:**

- Power:** The module is powered by a +3V supply and connected to GND.
- BT Module:** A BT module is connected to the module's pins. Its pins are labeled: BT\_+, BT\_-, BT\_+, BT\_-, BT\_+, BT\_-, BT\_+, BT\_-, BT\_+, BT\_-, BT\_-.
- BT Module Pins:** The BT module has two sets of pins: BT\_+ (pins 1, 3, 5, 7, 9, 11) and BT\_- (pins 2, 4, 6, 8, 10, 12).
- Module Pins:** The module has two sets of pins: BT\_+ (pins 1, 3, 5, 7, 9, 11) and BT\_- (pins 2, 4, 6, 8, 10, 12).
- BT Module Pins:** The BT module has two sets of pins: BT\_+ (pins 1, 3, 5, 7, 9, 11) and BT\_- (pins 2, 4, 6, 8, 10, 12).

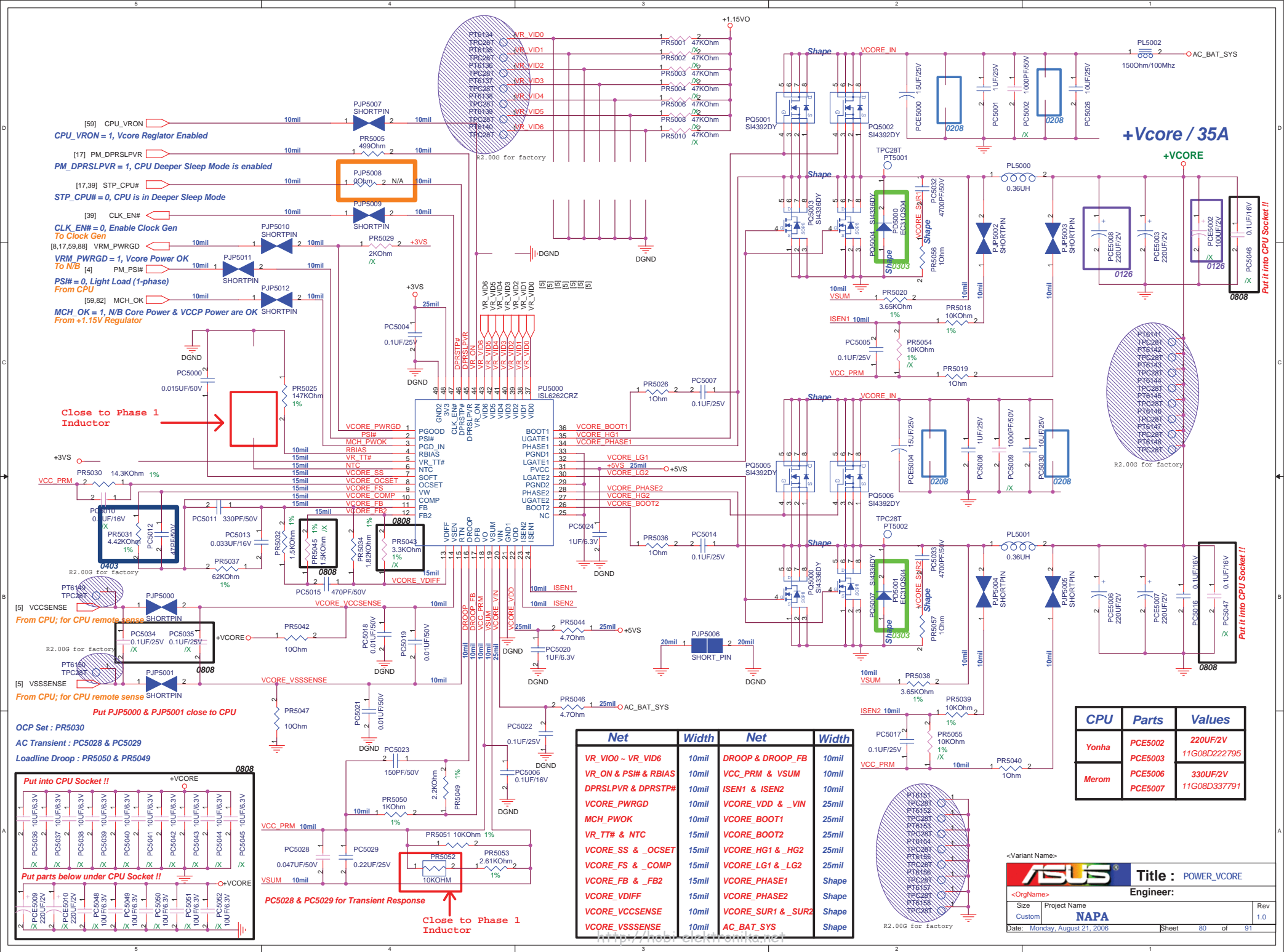
**Module Internal Circuitry:**

- Power Regulation:** A 3.3V regulator is shown, connected to the +3V supply and GND. The output of the regulator is connected to the module's +3V pin.
- Resistor:** A 10K resistor (R495) is connected between the +3V supply and the module's +3V pin.
- Transistors:** Two NPN transistors, Q73 and Q74, are used for switching. Q73 is connected to the BT\_ON/OFF# pin and the RF\_ON\_SW# pin. Q74 is connected to the BT\_ON pin.

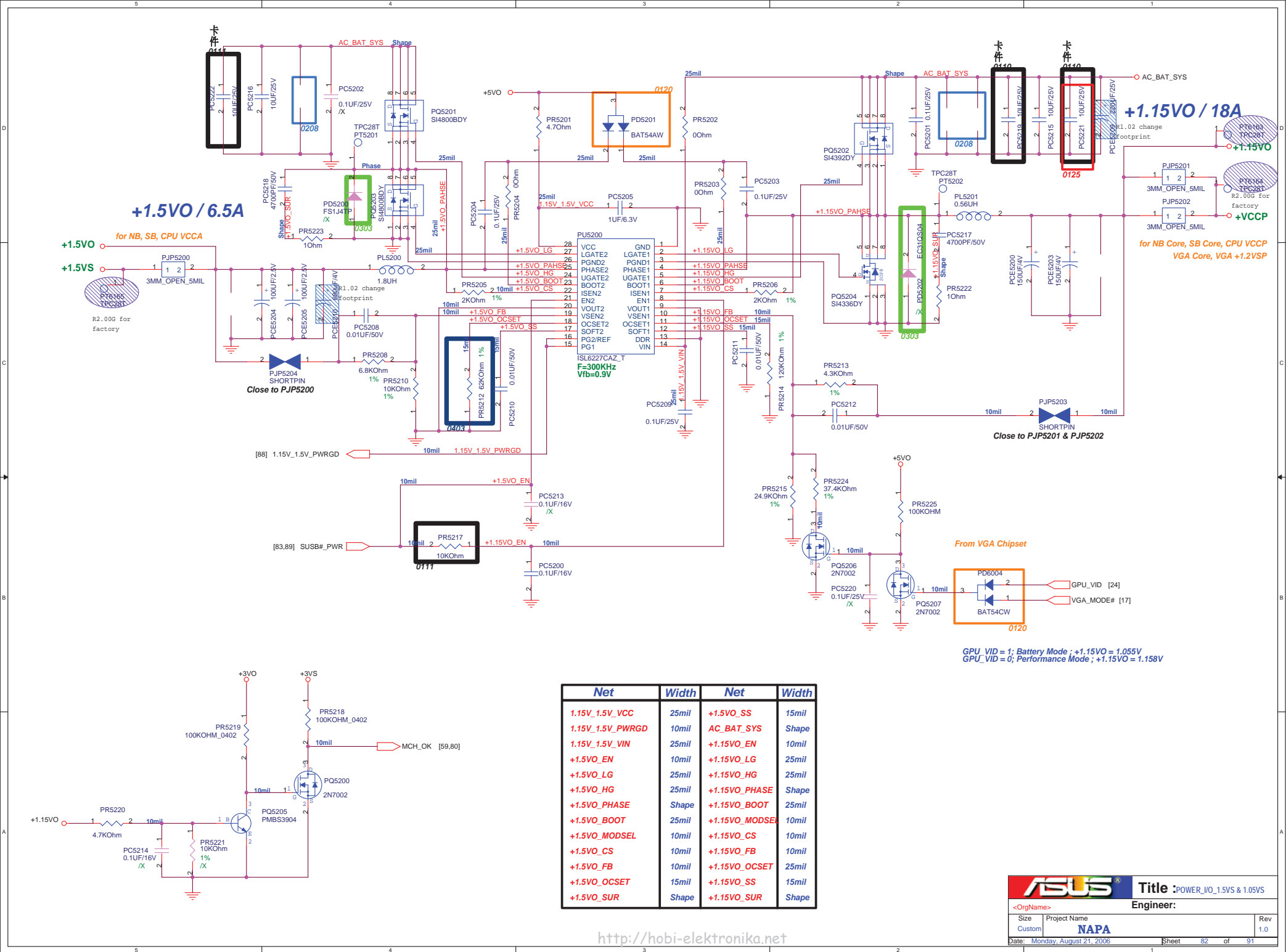


### For Side SW

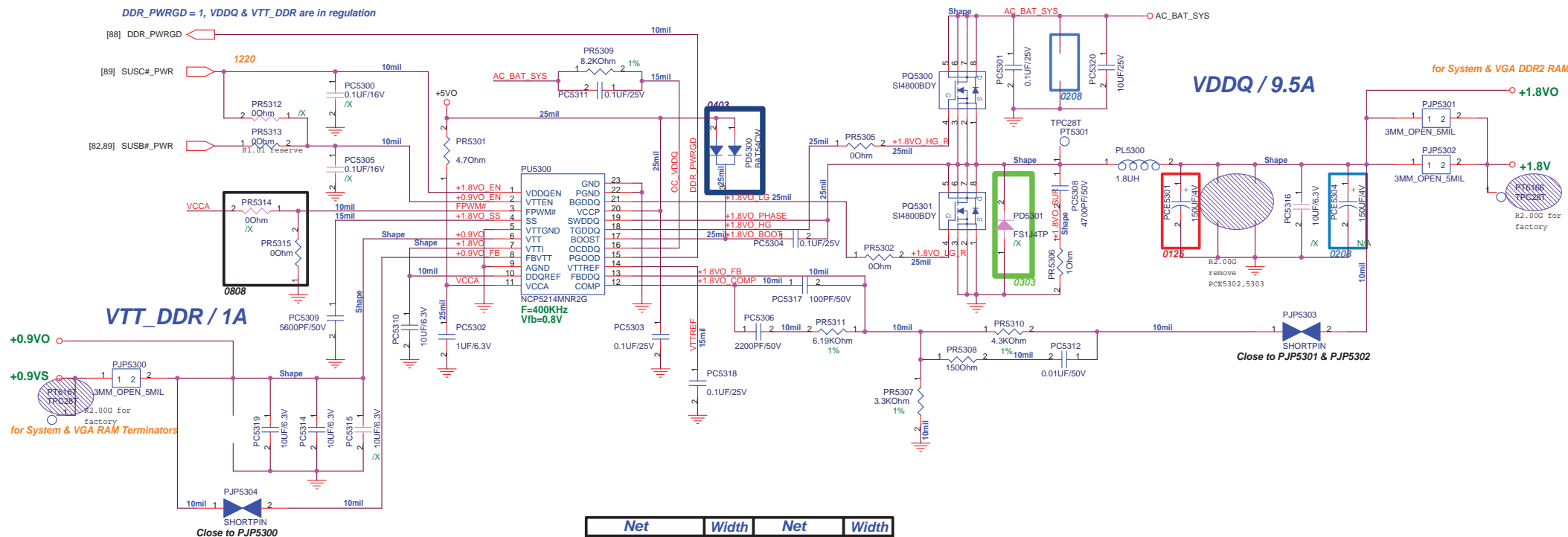
The diagram shows a circuit for a side switch. A +3V supply (labeled +3VA\_EC) is connected to a 10kΩ resistor (R493). The other end of R493 is connected to a node labeled [47,59] RF\_ON\_SW#. This node is also connected to a 330Ω resistor (R494) and a 0.1μF/16V capacitor (C665). The other end of R494 and one terminal of C665 are connected to a common GND plane. The other terminal of C665 is connected to a switch (SW10) labeled SLIDE\_SWITCH\_6P /X. The switch is connected to a GND plane. The switch has six terminals, with two connected to the GND plane and four connected to the RF\_ON\_SW# node.



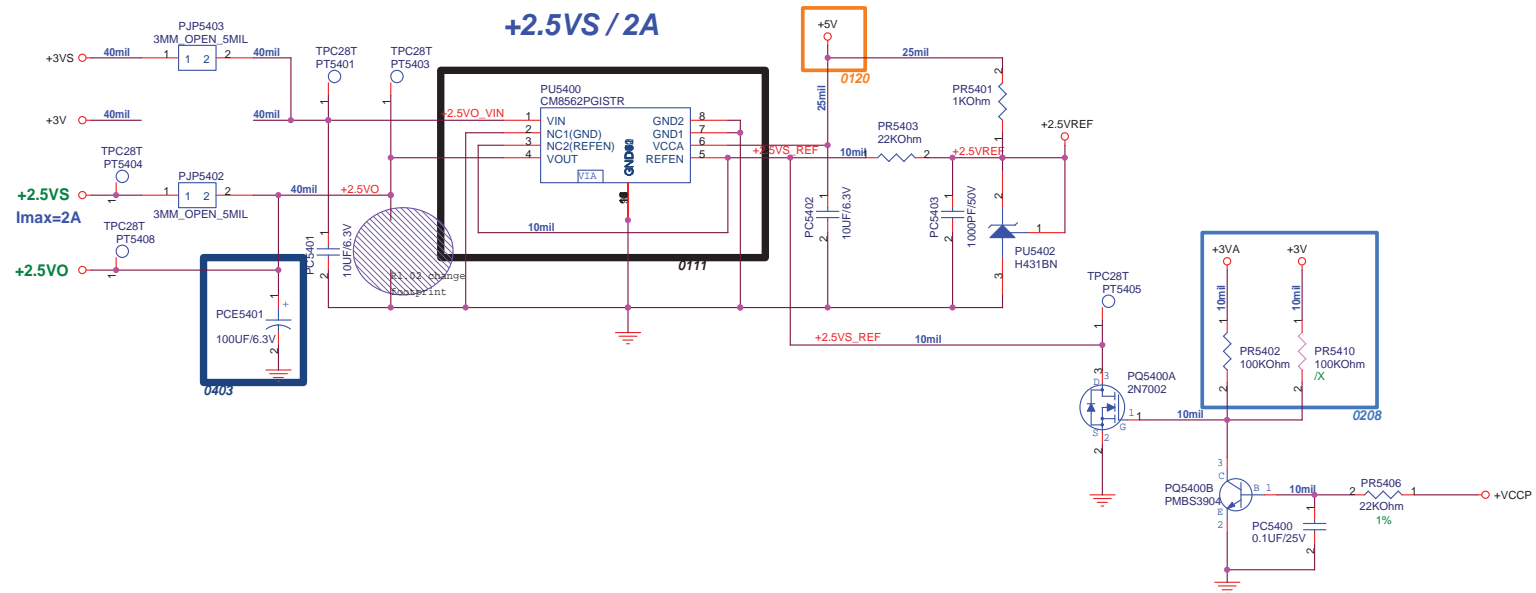
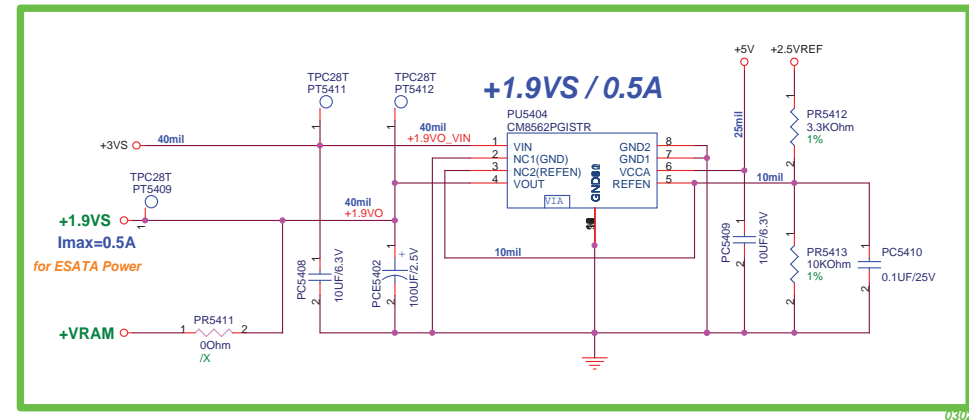
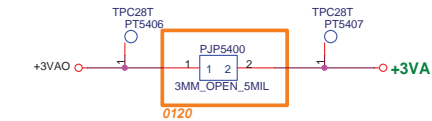
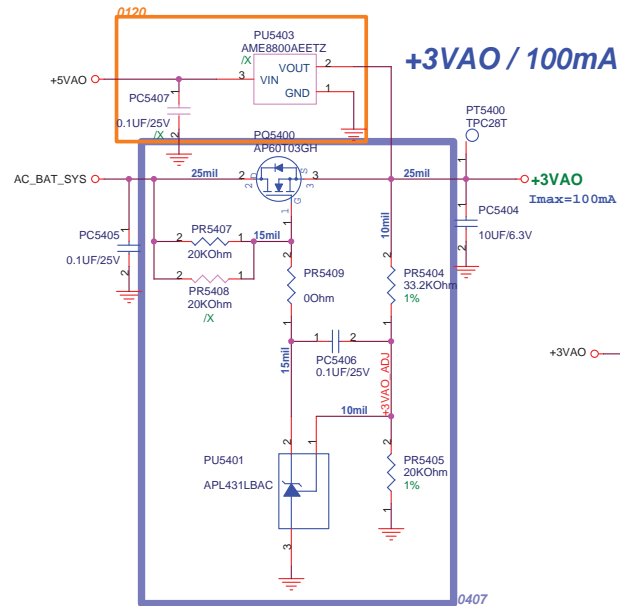






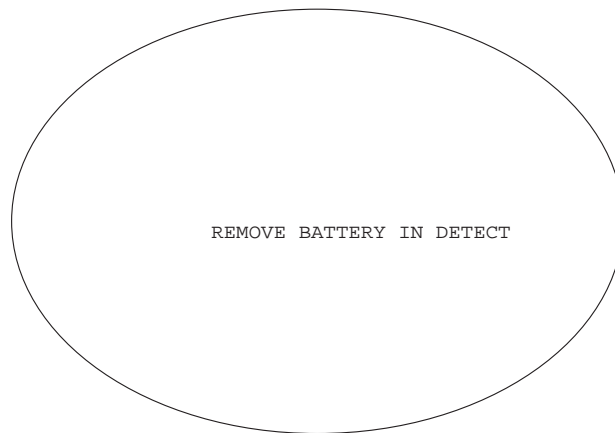


Net	Width	Net	Width
+1.8VO_EN	10mil	+1.8VO_BOOT	25mil
+1.8VO	Shape	+1.8VO_COMP	10mil
+0.9VO_EN	10mil	+1.8VO_HG_R	25mil
+0.9VO	Shape	+1.8VO_LG_R	25mil
+0.9VO_FB	10mil	+1.8VO_HG	25mil
+1.8VO --> DDQREF	10mil	+1.8VO_LG	25mil
VTTREF	15mil	+1.8VO_PHASE	Shape
FPWM#	10mil	+1.8VO_SUR	Shape
VCCA	10mil	+1.8VO_FB	10mil
DDR_PWRGD	10mil	+1.8VO_SS	15mil
OC_VDDQ	15mil	AC_BAT_SYS	Shape



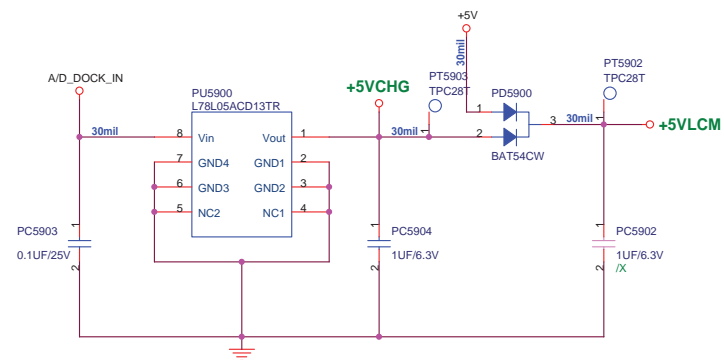




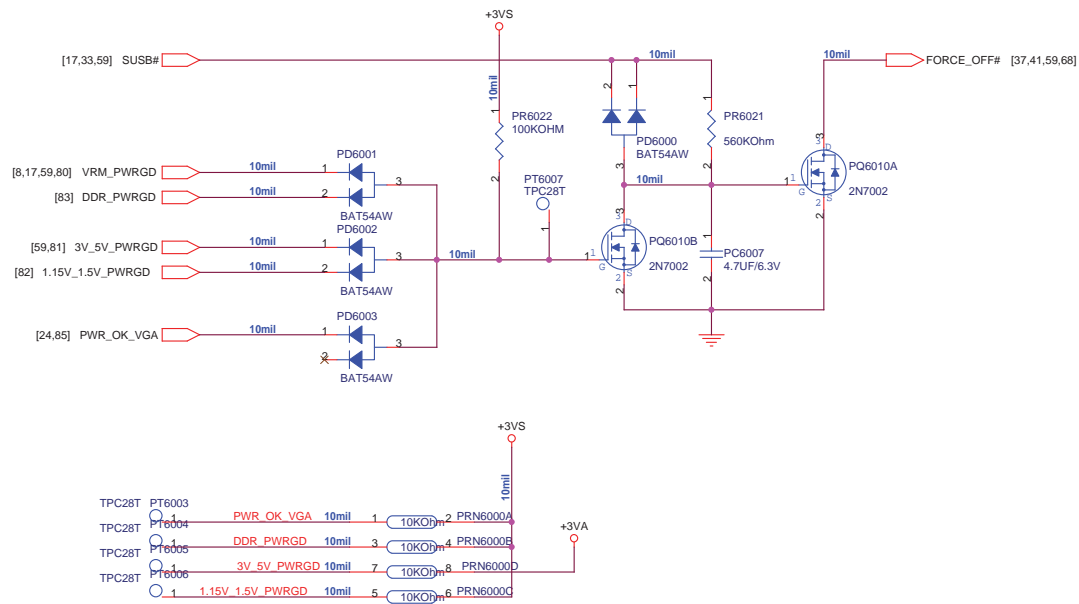


REMOVE BATTERY IN DETECT

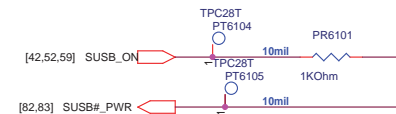
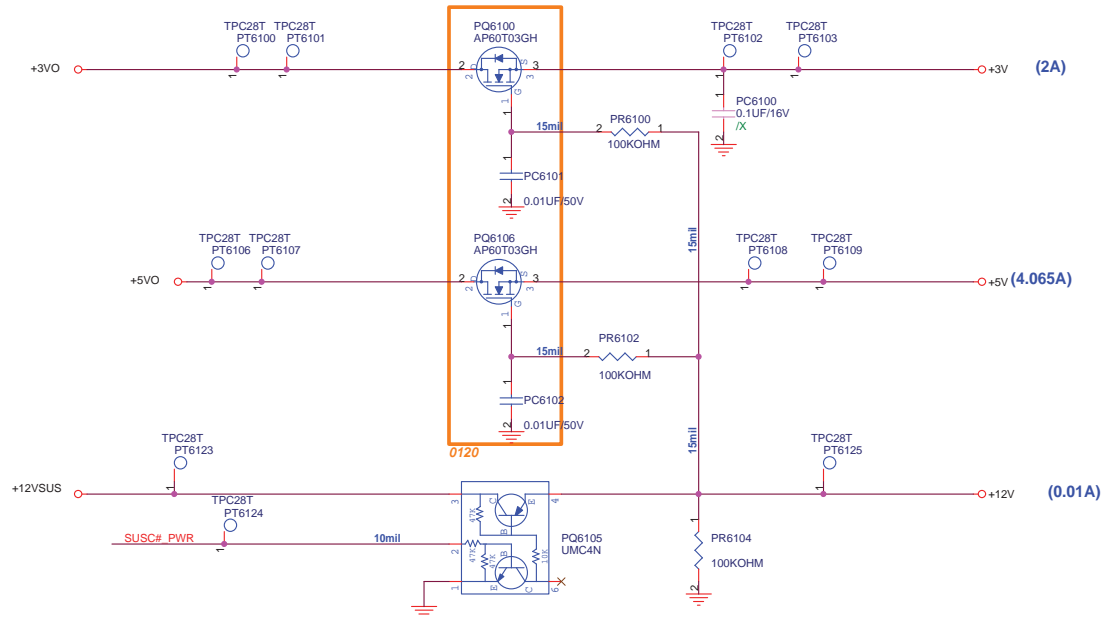
**+5VLCM / +5VCHG**



## Power Good Detector



## SUSC#\_PWR POWER



## SUSB#\_PWR POWER

